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A CMOS Transimpedance Amplifier Accommodating Wide C_{PD} and Input Bias Range for Chaos Lidar

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***Abstract*—This paper presents an input bias-adjustable and large-capacitance-tolerance transimpedance amplifier (TIA) for a chaotic light detection and ranging (Lidar) system. To cover the APD-bias adjustable range of ±0.5 V, a dual supply of 3.3/1.0 V that consumes 2.5/1.8 mA is used. In the 90-nm CMOS process, the TIA shows the 60-dBΩ gain and 450-MHz bandwidth. Its input-referred noise (IRN) is 61.3 pA/√Hz. This amplifier has been integrated into the prototyping system to generate the depth image with high detection accuracy.**

Keywords—CMOS transimpedance amplifier, light detection and ranging (Lidar), wideband circuit, shunt-feedback.

I. Introduction

The growing demands on autonomous vehicles, AR, and VR applications have driven the thriving development of ranging technology in recent years. Benefitting from the superior detection range and spatial resolution, Lidar is widely applied in object tracking, facial recognition, and environmental detection. Utilizing the time-of-flight (ToF) principle, Lidar acquires the distance information by measuring the phase shift or time difference between the emitted and reflected signal.

The conventional Lidar systems are vulnerable to crosstalk in multipath and multiuser scenarios. Although modulating the transmitted waveform with pseudo-random (PN) codes can mitigate the interference and jamming issues, pseudo-random modulation still encounters limitations like fake echoes due to its periodicity and regularity. The chaotic Lidar employing the nonlinear dynamics of semiconductor lasers exhibits noise-like waveform, flat power spectrum, and delta-like auto-correlation [1]. Its inherently aperiodic and unpredictable properties not only ensure the crosstalk immunity but also provide a low-cost alternative to tackle the interference problem.

In the application of depth imaging, a large-area photodiode (PD) is desired to expand the field of view (FoV) and the same time to increase the equivalent sensitivity for long-range detection. Depending on the detection range and FoV requirements, the PD size, and the associated parasitic, may vary over a wide range. For the wide FoV, long-range detection chaos Lidar system, we adopt an array structure to realize a large-area photodiode. The array structure is not only for scalability but also for the uniformity issues in PD. The mismatch between PD cells can be compensated by applying different biases for each cell.

For the pulsed chaos Lidar system, the TIA must meet the following requirements. Firstly, the amplifier must achieve the wide bandwidth of around 500 MHz to extract the high-speed chaos message. The transimpedance gain is 60 dBΩ. Noise performance is not stringent compared with the conventional ones because the PN-like code reduces the SNR requisition. The input node must accommodate a wide range of photo-detector size. The equivalent capacitance at input is targeted from 3 to 15 pF. At the same time, an input bias adjustable mechanism with ±0.5-V range is desired to compensate for the possible mismatches between each PD cell.

In the following, we will introduce our wideband TIA design for pulsed chaos Lidar in section II. The circuit realization and the optical-electrical performance in system integration will be revealed in section III. Conclusions will be drawn in the last section.

II. Proposed Circuit Architecture

A. Shunt-Feedback TIA with Common-Gate Input Stage

Shunt-feedback topology is widely applied in wideband transimpedance design [2] for its good compromise between each specification. For high-speed and low-noise purposes, a high-gain core amplifier with low power and low parasitic is preferred. Common source with dedicated gm-boosting techniques is widely used to achieve good figure of merit in speed and power efficiency. However, it is challenging to reach 60-dBΩ transimpedance gain and 500-MHz bandwidth with the input capacitance ranging from 3 to 15 pF.

Fig. 1 shows the circuit diagram of the proposed transimpedance amplifier. This TIA is composed of a shunt-resistor-feedback loop around a two-stage core amplifier. In the core amplifier, the first common gate, serving as the current buffer, is necessary to reduce the input impedance, to ensure stability when the input node with large capacitive loading. Moreover, the adjustability of input node voltage (V_{PD}) can be achieved by changing the voltage (V_{ADJ}). 3.3-V supply and the associated devices are used in this stage to accommodate ±0.5-V input voltage range for compensating the PD mismatches. The second common source stage provides the loop gain further. The 1-V devices are applied to reduce its power consumption and parasitic capacitance.

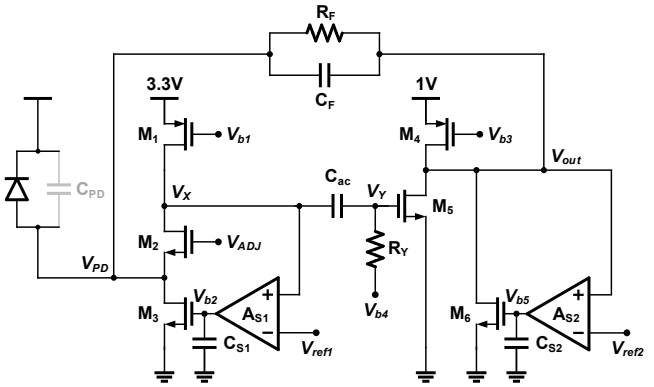

Fig. 1. Circuit diagram of the proposed CMOS transimpednace amplifier for the chaotic Lidar system.

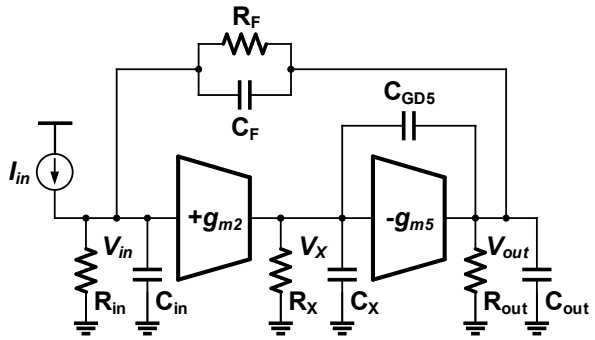

Fig. 2. The high-frequency equivalent model of proposed TIA.

The high-frequency characteristic of the proposed TIA can be simplified to the equivalent model depicted in Fig. 2. Based on the loop-breaking technique, there are three poles along the signal path. The open-loop poles can be derived as:

$$\omega_{p1} = \frac{-1}{(R_{in} \parallel R_F)C_{in}} \tag{1}$$

$$\omega_{p2} = \frac{-1}{R_X C_X} \tag{2}$$

$$\omega_{p3} = \frac{-1}{(R_{out} \parallel R_F)C_{out}} \tag{3}$$

where

$$R_{in} \approx \frac{r_{o2} + r_{o1}}{(g_{m2} + g_{mb2})r_{o2}} \parallel r_{o3} \tag{4}$$

$$R_X \approx (g_{m2} + g_{mb2})r_{o2}r_{o3} \parallel r_{o1} \tag{5}$$

$$R_{out} = r_{o4} \parallel r_{o5} \parallel r_{o6} \tag{6}$$

To estimate the loop stability, root locus is widely used by altering the loop gain and observing the pole location change. Fig. 3 shows the root locus of the proposed TIA circuit when the bridge capacitor C_F is nulled. By sweeping the feedback resistor R_F from 1 MΩ to 1 kΩ, the low-frequency poles become complex and move towards to the right-hand plane. It means that this three-pole system, without compensation, may be unstable with higher loop gain.

Before the system becomes unstable, the low-frequency complex-conjugate poles will make the frequency response with large peaking. In the time domain, this peaking will introduce extra ringing and then prolong the settling behavior. To alleviate these concerns, two design methods can be applied. The first approach is to push all the open-loop poles to high frequency and keep one as the dominant pole. Under our specific loop gain and high -3dB bandwidth, it is crucial to achieve this. The second method is using the compensation technique to alleviate the loop design difficulties.

In the proposed TIA, the compensation capacitor C_F is added. By KCL we can get the zero equation as in (7). There are two zeros. The LHP zero is helpful for stability, while the RHP zero is not welcome.

$$s^2 + \frac{(g_{m2} + g_{mb2})C_{GD5}}{C_F C_X}s - \frac{(g_{m2} + g_{mb2})g_{m5}}{C_F C_X} = 0 \tag{7}$$

We use the approximations, as shown in (8) and (9), to simplify the expression of zeros as (10).

$$g_{m2} \sim g_{m5} \tag{8}$$

$$C_X \sim C_F \gg C_{GD5} \tag{9}$$

$$\omega_{z1,2} = \pm\sqrt{\frac{(g_{m2} + g_{mb2})g_{m5}}{C_F C_X}} \tag{10}$$

Fig. 4 shows the zero location movement when sweeping C_F from 0 to 220 fF and keeping 1-kΩ R_F unchanged. With larger C_F, two zeros will walk to low frequency. Fig. 5 shows the closed-loop pole movement when the compensation C_F is inserted. The LHP zero pulls the complex poles ω_{p1} and ω_{p2} leftwards to improve speed and stability with no power penalty. But the RHP zero also pulls high-frequency pole ω_{p3} rightwards to low frequency. In this design, the value of C_F is selected as 220 fF to get a good trade-off between power, speed, and stability.

Additionally, to tolerate the input capacitance from 3 to 15 pF, we design the input node always serve as the dominant pole. This strategy maintains consistent open-loop and closed-loop characteristics across varying input loads. The proposed TIA, designed for 15 pF with 450-MHz bandwidth and 70-degree phase margin, guarantees the speed and stability at the 3-pF condition, as shown in Table I.

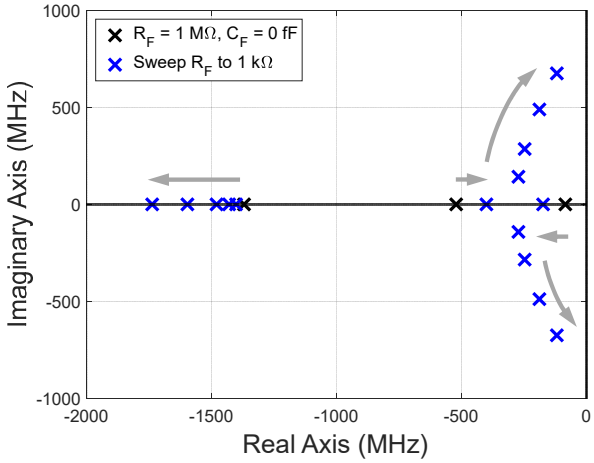

Fig. 3. Movement of closed-loop poles while C_F is 0 fF and R_F is swept from 1 MΩ to 1 kΩ.

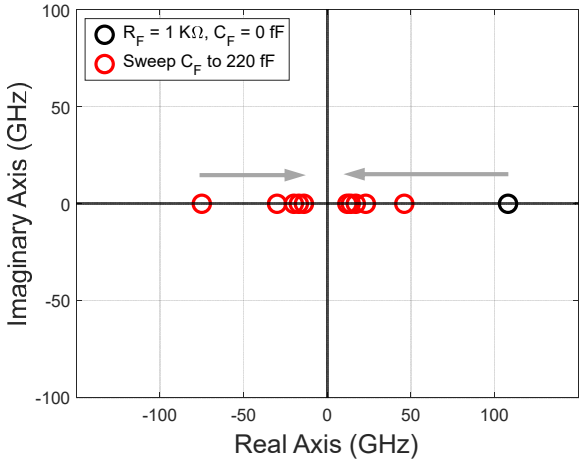

Fig. 4. Zero movement when C_F is from 0 to 220 fF.

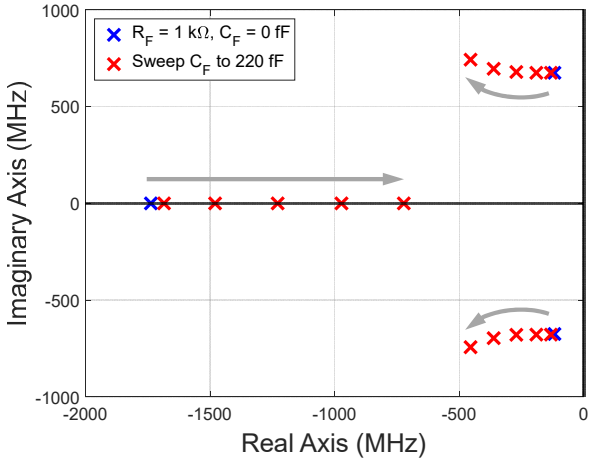

Fig. 5. The closed-loop pole location when C_F is swept from 0 to 220 fF while keeping R_F is 1 kΩ.

TABLE I. TIA PERFORMANCE ACROSS VARYING INPUT LOADS

Cin (pF)	3	6	9	12	15
BW (MHz)	509	527	516	489	457
PM (deg.)	64	66	68	70	72
Tsettle,rise (ns)	1.48	1.56	1.66	1.76	1.9
Tsettle,fall (ns)	1.54	1.51	1.46	1.37	1.37

B. Input Node Bias-Adjustable Mechanism

The common-gate topology is adopted as the first stage of the core amplifier. This input stage, as shown in Fig. 1, can sustain the input impedance minimization. Furthermore, this arrangement is beneficial to integrate the function of input bias voltage adjustment. When the bias current of M_1 and M_2 is fixed, ideally the gate-to-source voltage of M_2 is constant. We can set different voltages at node V_{ADJ} to make the input node V_{PD} follow the change. In the front-end array, each PD bias voltage can be individually adjusted at the V_{ADJ} node to compensate for the mismatch. The tuning range has to be larger than ±0.5 V, since from the measurement data, the in-house PD with a large size suffers a certain mismatch.

Considering the channel length modulation and body effect, the current of M_1 and M_2 is no longer kept with the design value when input bias voltage changes. To guarantee that the operation points are stable, both in the first and second gain stages, DC-stabilization loops are incorporated. In the low-frequency range of Fig. 6, the blue and red lines depict the open-loop frequency responses of the first stage and the second stage control loop. In our design, the gains of the two loops are similar. But the -3dB corner frequency of the first stage is around two orders smaller than the that of the second stage. This arrangement avoids the frequency peak when the global shunt-feedback loop is connected. The settling can be smoother since less interaction between the two loops. The black curve in Fig. 6 shows the overall TIA frequency response. With two DC-stabilization loops, the sensitivity of input DC bias can be greatly reduced. The signal band designed is between 100 KHz and 450 MHz for 100-ns pulses with fast chaos information embedded.

III. MEASUREMENT RESULTS

Fig. 7 shows the prototype chip with 8 TIA channels integrated. It is implemented in the 90-nm CMOS with mixing 3.3-V devices at the input stage and 1-V devices for the rest. The active area of the core TIA circuits is around 0.01 mm^2. For ease of system integration, the bias of each amplifier is adjusted externally in this version. The pin number can be reduced by an integrated bias control. Fig. 8 is the equivalent network to emulate the input photocurrent for electrical testing. R_L is an impedance match to the source equipment. R_H and C_a serve as the current conversions. Different C_S is used to evaluate the circuit performance under the parasitic capacitance of various APD sizes.

Fig. 9 shows the frequency response of the proposed transimpedance amplifier with electrical current input. Three curves indicate that the transimpedance gain under different input bias voltage settings remains 56 dBΩ. They come from 60 dBΩ by the amplifier and 4-dBΩ loss by an output buffer. The -3dB bandwidth is around 450MHz. The amplifier proposed is integrated with an in-house APD on PCB. The APD is driven by a chaotic laser system. The setup is shown in Fig. 10(a). Fig. 10(b) is the TIA output time-domain waveform. Within 100-ns Lidar impulse, the nanosecond chaotic signal can be successfully detected.

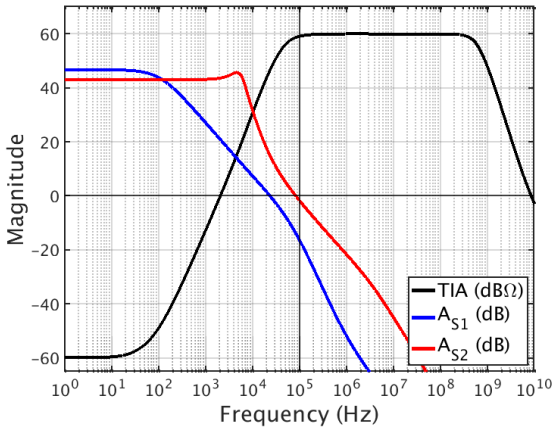

Fig. 6. Closed-loop frequency response of the overall TIA and the open-loop response of two DC stabilization loops with amplifiers A_{S1} and A_{S2}.

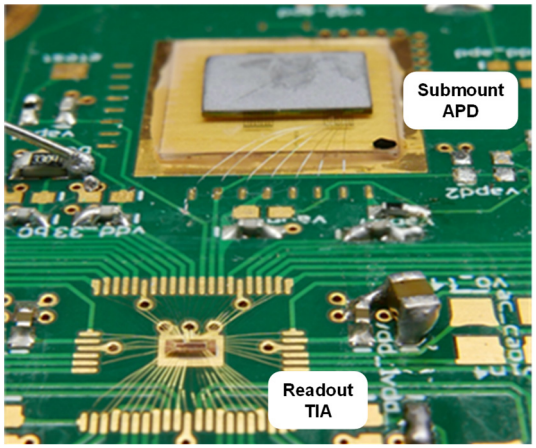

Fig. 7. The prototype chip with 8 TIA channels connected to the in-house submount APD.

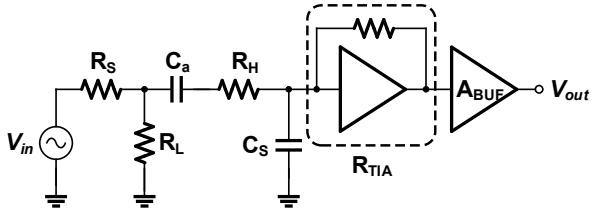

Fig. 8. Input network and output buffer for TIA electrical tests.

A chaotic Lidar prototype with the proposed trans-impedance amplifier, an in-house array APD and a mixed-signal ToF detector [3] are built up to verify its performance. Fig. 11 shows the system block diagram, and the maximum error within the detection range of 45 to 180 cm is ±4 cm. Table II compares the TIA designed for various applications. As mentioned, the depth imaging requires wide FoV and thus large photodetector. To overcome the 15-pF input capacitance, the common-gate topology is employed in our first stage. Although our proposed TIA increases the input-referred noise than [5], [6] whose first stage utilizes the common-source topology, it supports the input-bias adjustable mechanism to compensate the mismatch between PD cells.

IV. Conclusion

This work develops a wideband CMOS transimpedance amplifier for chaos Lidar front-end requirements. Shunt-feedback topology with a two-stage common-gate-common-source amplifier achieves a wide while stable bandwidth with large tolerance on input capacitance and input bias condition. The verifications, besides in the electrical domain, optical-electrical integration is accomplished to evaluate the pulsed chaos Lidar system.

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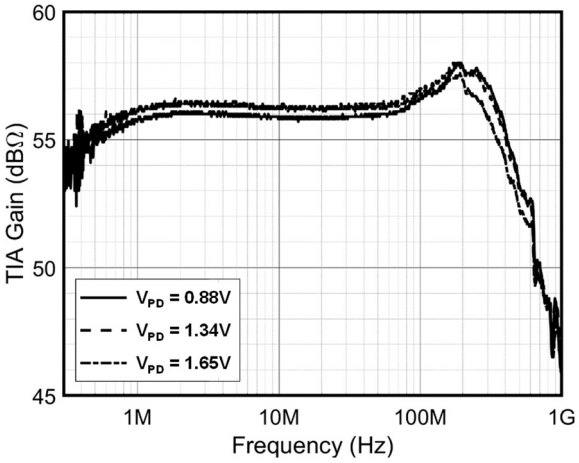

Fig. 9. Frequency response of the proposed TIA under three different input bias voltages.

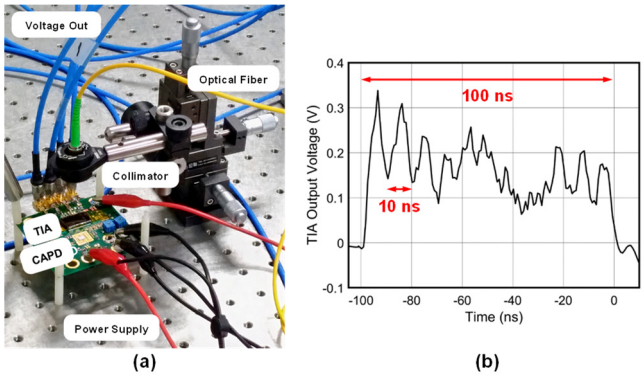

Fig. 10. The setup for the optical-electrical test. (b) the output waveform of the amplified chaotic signal.

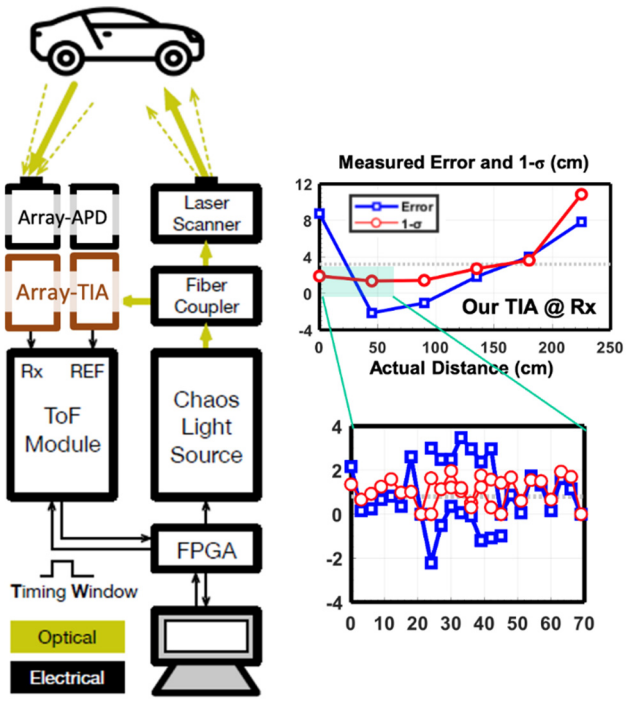

Fig. 11. The chaotic Lidar prototype system [3] and its maximum error of ±4 cm within the detection range of 45 to 180 cm.

TABLE II. TIA Performance Summary and Comparison

Ref.	TCAS-I'16 [4]	TVLSI'24 [5]	TCAS- I'21 [6]	This work
CMOS Tech.	130nm	180nm	110nm	90nm
Application	Optical Comm	FMCW Lidar	Pulsed Lidar	Chaos Lidar
Supply (V)	1.2	3.3	1.8	3.3/1
Current (mA)	8	15.6	10.8	2.5/1.8
Power (mW)	9.6	51.5	19.4	10.1
CKT Topology	Dual FB	Shunt FB	Shunt FB	Shunt FB
Gain (dBΩ)	40	107	94	60
BW (MHz)	2500	165	340	450
C_{PD} (pF)	15	2	1	3 to 15
IRN (pA/√Hz)	240	2.29	3.67	61.3
Input Bias Adj	No	No	No	±0.5 V

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