A 56-Gb/s PAM-4 Optical Transceiver with Nonlinear FFE for VCSEL Driver in 40nm CMOS

Pen-Jui Peng[1], Hsiang-En Huang[2], Wei-Chien Huang[2], Po-Lin Lee[2], Ming-Wei Lin[3], Ying-Zong Juang[3], Sheng-Hsiang Tseng[3]

[1]National Tsing Hua University, Hsinchu, Taiwan

[2]Yuan Ze University, Taoyuan, Taiwan

[3]Taiwan Semiconductor Research Institute, Hsinchu, Taiwan

2021 IEEE Asian Solid-State Circuits Conference (A-SSCC) | 978-1-6654-4350-0/21/$31.00 ©2021 IEEE | DOI: 10.1109/A-SSCC53895.2021.9634783

This paper presents a 56Gb/s PAM-4 optical transceiver fabricated in 40nm CMOS. Differing from the optical transmitters with microring [1] or Mach-Zehnder [2] modulators that require high voltage swing to drive, the VCSEL can be directly driven by a small current, making a power-efficient solution for short reach application (<100m) through the multimode fiber. The optical TX adopts a DAC-based structure with a 2-tap nonlinear PAM-4 FFE implemented in the DSP domain to compensate for the VCSEL's asymmetric responses. For the optical receiver, it accommodates an external PD+TIA with the electrical RX, increasing the flexibility for system applications. The VCSEL transmitter demonstrates a 56Gb/s compensated PAM-4 waveform with −0.9dBm outer OMA while consuming only 97mW of power (1.73pJ/b). The RX achieves 10^{-12} BER with 0.08UI margin under 10dB interconnection loss between the PD+TIA module and the RX chip while dissipating 278mW of power (4.96pJ/b).

Fig. 1 illustrates the 56Gb/s PAM-4 VCSEL transmitter architecture which incorporates a 7b DAC with a two-tap non-linear FFE implemented in the DSP domain. The 7b DAC adopts a segmented structure with 5 binary slices controlled by binary code and 3 unary slices controlled by thermometer code to reduce the nonlinearities [3]. After serializing by the following 64:8 MUX, 8:4 MUX, and 4:1 MUX, the 56Gb/s data goes through the current-mode driver to accomplish the current combination with the 50Ω loads. One of the differential output connects to the external VCSEL through a wirebond with a biasing current I_{TH} to reduce the switching time. The terminated driver topology reduces the reflection due to the impedance mismatch on either side of the wirebond channel. The VCSEL suffers from nonlinear responses at different bias current, resulting in asymmetric responses between "zero" pulse and "one" pulse. To deal with the nonlinearity, the asymmetric FFE has been adopted in [4] by separating the input into rising and falling pulses and adjusting the weights independently. This phenomenon becomes more serious in PAM-4 signaling due to its multiple data transitions and could not be easily compensated by rising and falling pulses. In this work, the nonlinear FFE is implemented in the digital domain by using a look-up table (LUT) for the FFE coefficients and pre-selected according to the present and the next symbols. Moreover, the RLM of the PAM-4 signal can be optimized since each level can be adjusted independently. To reduce the clocking power, 2UI pulses rather than 1UI pulses are utilized by selecting the input data with one zero-crossing in the center as shown in the timing diagram in Fig. 1. Phase interpolators (PIs) are used to adjust the data delay and work together with the DCCs/QECs for minimizing the periodical jitter.

Fig. 2 shows the architecture of the 56Gb/s PAM-4 optical RX. After captured by the external PD+TIA, the optical signal is then transferred into voltage and fed into the RX chip through a chip-on-board (COB) assembly. The RX includes the CTLE and the 1-tap DFE to compensate for the interconnection loss. To increase the dynamic range and maintain the linearity of the PAM-4 signal, 2 VGAs are put in the front-end with −10~10dB tunable gain to provide appropriate swing for the following half-rate DFE summers. After eliminating the 1st post-cursor by the DFE summer, the PAM-4 signal is sampled by 3 data slicers, 1 error slicer, and 1 edge slicer. The data slicers resolve the PAM-4 signal into 3b thermometer code with 3 independently adaptive reference voltage created by the DAC array, minimizing the BER degradation due to the nonlinearity of the PAM-4 signal. After transferred into binary code (MSB and LSB) by the thermometer-to-binary decoder, the data, error, and edge samples are aligned and de-multiplexed to the digital circuit for adaptation loops of DFE, reference, and CDR. The schematic of the slicer is also shown in Fig. 2, which incorporates a double-tail sense amplifier with subtraction in the first stage. To resist the stringent timing constraint from the 1-tap DFE, the RZ signals are directly used to reduce the feedback delay. Isolated inverters INV_1 and INV_2 are used to provide RZ signals H_1 for the 1-tap DFE summer and help to separate the load effect from the SR latch. Finally, a 4-tap FFE TX is included in the RX to recover and deliver the pure PAM-4 waveform, forming a complete 56Gb/s PAM-4 retimer.

The 4-tap FFE TX architecture is depicted in Fig. 3. It consists of 3.5, 7.5, 7.5, 3.5 slicers for the pre-, main-, 1st post-, and 2nd post-cursors, respectively. Each slice includes 3 identical structures divided into MSB and LSB paths with coefficient MUXs to adjust the amount of equalization. After aligned and skewed by the retiming latches, the half-rate data are serialized into the full-rate output by the 2:1 MUX which is merged with the voltage-mode driver to obviate the predriver, making a power-efficient design.

Both the TX and RX are fabricated in 40nm CMOS technology. The TX consumes a total power of 93mW from 0.9V (core), 1.2V (driver), and 3V (VCSEL) supplies, while the RX dissipates a total power of 278mW (excluding the 4-tap FFE driver) from a 1.2V supply. Fig. 4 shows the TX measurement results. The electrical eye diagram achieves a $300mV_{ppd}$ output swing with 64mV minimum eye-opening. The frequency response of the VCSEL is also recorded, suggesting asymmetric responses under different bias current. The measured −3dB bandwidth varies from 14 to 17GHz with unwanted peaking which needs to be compensated by the nonlinear FFE. The optical output waveforms are captured as well, which are directly received through a bare multimode fiber with approximately 3dB coupling loss. After optimizing the coefficients of the nonlinear PAM-4 FFE, a symmetric PAM-4 eye diagram can be observed with the de-embedded OMA of −0.9dBm.

Fig. 5 shows the 56Gb/s RX measurement results. The TIA's output achieves $120mV_{ppd}$ output swing under −3dBm OMA input. The overall Nyquist loss from the package of PD+TIA and the interconnection to the COB-assembled RX chip is roughly 10dB. The RX bathtub under different equalization is also shown in Fig. 5. After compensating by the CTLE and 1-tap DFE, the RX achieves BER of 10^{-12} with a 0.08UI margin. The recovered 56Gb/s PAM-4 output waveform is recorded, implying $700mV_{ppd}$ swing with negligible ISI compensated by the 4-tap FFE. The RX jitter tolerance (JTOL) with a 10^{-6} confidence level is also shown in Fig. 5, which meets the JTOL mask defined by IEEE 802.3bs [5].

Fig. 6 summarizes the performance of this work with other state-of-the-arts recently published. The die photographs are shown in Fig. 7, which occupy active areas of $0.85x0.55mm^2$ for TX and $0.66x0.5mm^2$ for RX, respectively. The detailed power breakdowns are recorded in Fig. 7 as well.

References:

[1] H. Li *et al.*, "A 3D-Integrated Microring-Based 112Gb/s PAM-4 Silicon-Photonic Transmitter with Integrated Nonlinear Equalization and Thermal Control," *ISSCC Dig. Tech. Papers*, pp. 208-209, Feb. 2020.

[2] E. Sentieri *et al.*, "A 4-Channel 200Gb/s PAM-4 BiCMOS Transceiver with Silicon Photonics Front-Ends for Gigabit Ethernet Applications," *ISSCC Dig. Tech. Papers*, pp. 210-211, Feb. 2020.

[3] C. Menolfi *et al.*, "A 112Gb/s 2.6pJ/b 8-Tap FFE PAM-4 SST TX in 14nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 104-105, Feb. 2018.

[4] M. Raj, M. Monge, A. Emami, "A Modelling and Nonlinear Equalization Technique for a 20 Gb/s 0.77 pJ/b VCSEL Transmitter in 32 nm SOI CMOS," *IEEE Journal of Solid-State Circuits*, vol. 51, pp. 1734-1743, Jul. 2016.

[5] IEEE P802.3bs 400GbE, <http://www.ieee802.org/3/bs/>

[6] J. Jiang *et al.*, "100Gb/s Ethernet Chipsets in 65nm CMOS Technology," *ISSCC Dig. Tech. Papers*, pp. 120-121, Feb. 2013.

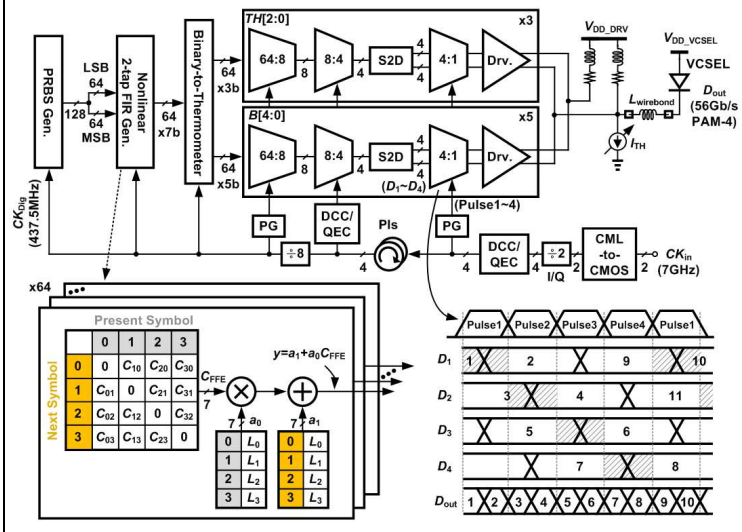

Fig. 1. TX architecture.

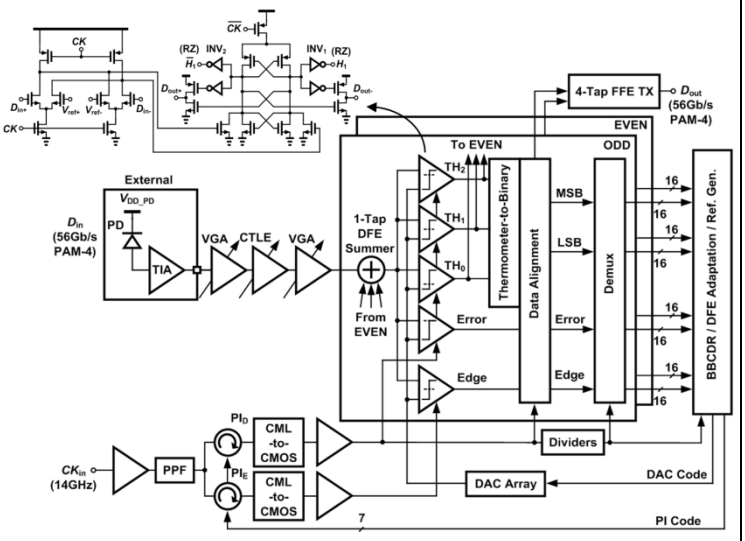

Fig. 2. RX architecture.

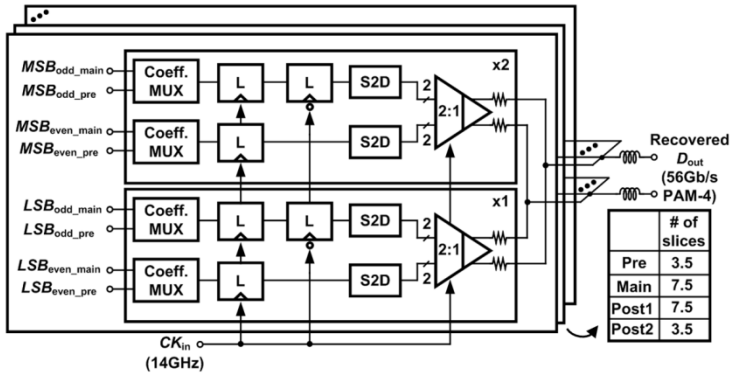

Fig. 3. 4-tap FFE TX architecture.

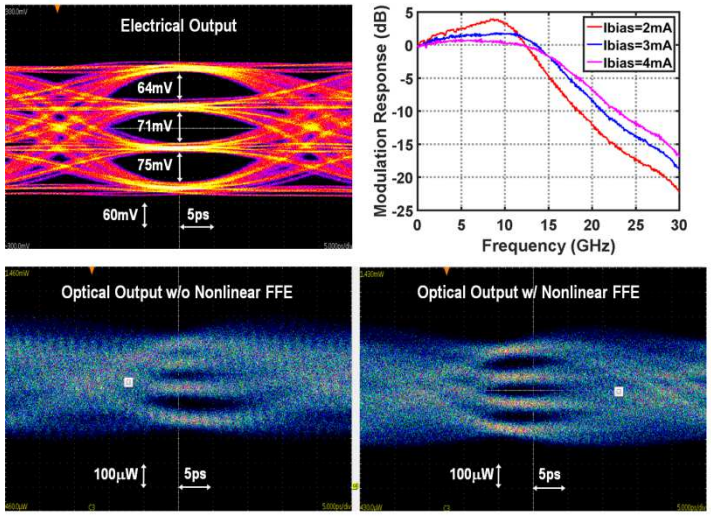

Fig. 4. Transmitter measurement results: TX electrical eye diagram at 56Gb/s (top left), VCSEL modulation response (top right), TX optical eye diagrams at 56Gb/s without (bottom left) and with nonlinear FFE (bottom right).

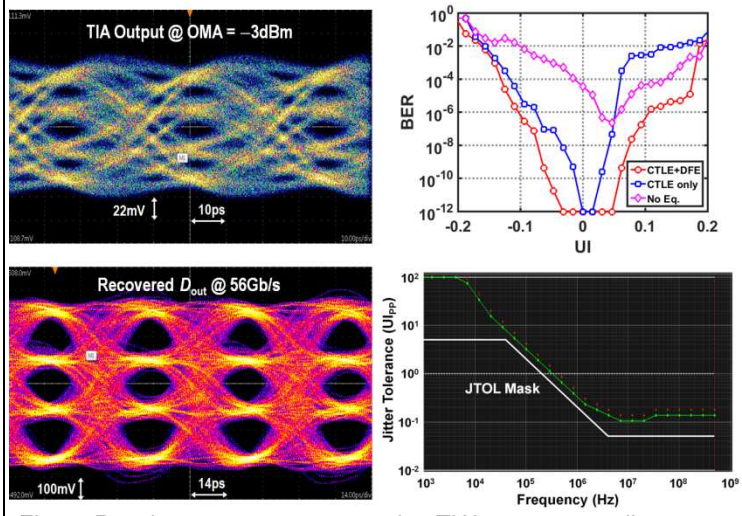

Fig. 5. Receiver measurement results: TIA's output eye diagram at 56Gb/s (top left), RX bathtub (top right), recovered data (bottom left), and RX jitter tolerance (bottom right).

Optical TX	[6] ISSCC '13	[7] VLSI '19	This Work
FFE Topology	Symmetric	Asymmetric for MSB/LSB	Asymmetric for all traces
Data-rate (Gb/s)	25	64	56
Signaling	NRZ	PAM-4	PAM-4
OMA (dBm)	0.79	3.98	−0.9
Serialization Ratio	1:1	8:1	64:1
Power Consumption (mW)	99	147	97
Efficiency (pJ/bit)	3.96	2.29	1.73
Core Area (mm^2)	0.5	0.278	0.468
Technology	65nm CMOS	65nm CMOS	40nm CMOS

RX	[8] ISSCC '17	[9] ISSCC '17	This Work
Function	CTLE + 3-tap DFE + CDR	CTLE + 10-tap DFE + CDR	CTLE + 1-tap DFE + CDR
Data-rate (Gb/s)	56	56	56
Channel Loss	24dB @ 14GHz	10dB @ 14GHz	10dB @ 14GHz
BER	10^{-12}	10^{-12}	10^{-12}
Power Consumption (mW)	382	230	278
Efficiency (pJ/bit)	6.82	4.1	4.96
Core Area (mm^2)	1.26	0.364	0.33
Technology	40nm CMOS	16nm FinFET	40nm CMOS

Fig. 6. Performance summary.

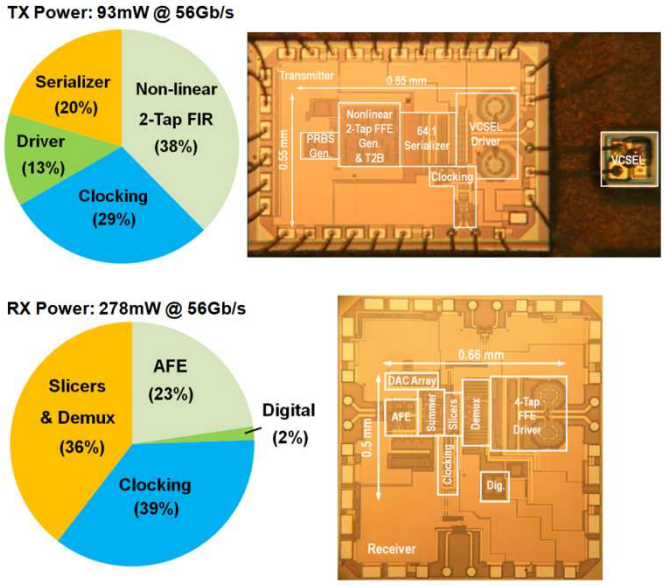

Fig.7. Die photographs and detailed power breakdowns.

Additional References:

[7] J. Hwang *et al.*, "A 64Gb/s 2.29pJ/b PAM-4 VCSEL Transmitter With 3-Tap Asymmetric FFE in 65nm CMOS," *Digest of Symposium on VLSI Circuits*, pp. 268-269, Jun. 2019.

[8] P. Peng *et al.*, "A 56Gb/s PAM-4/NRZ Transceiver in 40nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 110-111, Feb. 2017.

[9] J. Im *et al.*, "A 40-to-56Gb/s PAM-4 Receiver with 10-Tap Direct Decision-Feedback Equalization in 16nm FinFET," *ISSCC Dig. Tech. Papers*, pp. 114-115, Feb. 2017.