A Wideband Low-Noise Linear LiDAR Analog Front-End Achieving 1.6 GHz bandwidth, 2.7 pA/Hz$^{0.5}$ Input Referred Noise, and 103 dBΩ Transimpedance Gain

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Linear LiDAR can obtain distance by measuring time of flight (TOF), which is widely used in unmanned, geomorphic mapping and other fields. In recent years, the demand of long-distance LiDAR is getting increased. The maximum detection range of pulsed LiDAR is mainly dictated by the signal-to-noise ratio (SNR) [1]. Fig.1 (top) indicates that improving the SNR relies on enhancing the peak emission power of the laser pulse and reducing the noise of the analog front-end (AFE) circuit. Moreover, to comply with safety regulations for eye-safe laser energy [1], narrow high-power laser pulse is required. Since the pulse width of high-power laser has already reached sub-nanosecond range [2], an AFE with a wide bandwidth of over-1 GHz and lower noise is required, thus significantly challenging the circuit design. In the AFE, the input referred noise (IRN) is mainly dominated by the transimpedance amplifier (TIA). Prior shunt-feedback TIA (SF-TIA) [3] performs well with a narrow bandwidth around 100 MHz. But it suffers from strong trade-off between IRN, gain, bandwidth and stability. Thus, the IRN is higher than 4.5 pA/Hz$^{0.5}$ with over-200-MHz bandwidth [4, 5], indicating unsuitable for the design of low-noise TIA with over-1-GHz bandwidth and high gain. A low IRN of 2.6 pA/Hz$^{0.5}$ was achieved by using a narrow-band TIA along with an equalizer for bandwidth enhancement (190 MHz) [6]. But this is still not sufficient for the design of over-1-GHz TIA.

This paper presents an AFE circuit for linear LiDAR scoring a wide bandwidth of 1.6 GHz and a low IRN of 2.7 pA/Hz$^{0.5}$ with a gain of 103 dBΩ concurrently, as the block diagram illustrated in Fig. 1 (bottom). The NMOS feedforward TIA with inner feedback resistor (NFFR-TIA) is devised to mitigate the design trade-offs of prior SF-TIAs, thus achieving wide bandwidth around 400MHz with low IRN and high gain. Two stage continuous-time linear equalizers (CTLE) are utilized to further boost the bandwidth to 1.6 GHz with a flatten in-band AC response and without IRN degradation.

The widely used SF-TIA is depicted in Fig. 2 (top), which suffers from strong trade-offs between bandwidth, IRN, stability and gain: using a large feedback resistor R_f reduces IRN but comes with low bandwidth; a TIA with high open-loop gain A_0 helps to ensure sufficient bandwidth, yet, it may degrades stability; a feedback capacitor C_f improves the stability [3] whereas it increases equivalent input capacitance of the TIA, thus degrading bandwidth.

To surmount these issues, we propose the NFFR-TIA, as the detailed schematic shown in Fig. 2 (bottom). The three-stage cascade topology is used to enhance open-loop gain for wideband design consideration. To solve the stability issue of the conventional SF-TIA with high open-loop gain, we introduce an NMOS feedforward stage, which consists of a NMOS M_L and a resistor R_L (R_L can avoid oscillation caused by the inductance of the input bonding wire). This reduces the output resistance by paralleling M_L to increase the non-dominant pole, thus improving the phase margin for better stability. Meanwhile, using the feedforward M_L also reduces the input resistance of the TIA, leading to higher bandwidth with the same feedback resistance R_{F1}. This indicates that both lower IRN and higher bandwidth can be achieved concurrently by properly setting R_{F1}, compared to the conventional SF-TIA. To further suppress IRN, the first stage of the NFFR-TIA core amplifier is designed with a high transconductance.

The gain of the TIA should be adjustable with sufficient tuning range to meet the requirement of measuring different distances. The is performed by tuning the resistance of feedback resistor R_f in the conventional SF-TIA. However, in our case of three-stage TIA, if reducing R_{f1} at low-gain mode, the bandwidth gets increased, thus causing stability issue due to the fixed value of the non-dominant poles at the inner nodes of the TIA (see node A and B in Fig. 2 (bottom)). So, to mitigate this issue, we introduce a tunable feedback R_{F2} in the second stage of this NFFR-TIA, and R_{F1} and R_{F2} are tuned simultaneously. At low gain mode, both R_{F1} and R_{F2} are adjusted to a small value; thus, the poles at node A and B are increased due the reduced resistances of node A and B with lower R_{F2} to ensure the stability. At high gain mode, both R_{F1} and R_{F2} are increased to obtain a sufficient open-loop gain.

The NFFR-TIA can improve the bandwidth to near 400 MHz with a low IRN of 2.0 pA/Hz$^{0.5}$ according to the post-layout simulation results. Yet, this is still far away from our design target of over-1-GHz bandwidth. Therefore, we employ two stage CTLEs to further improve the bandwidth, as illustrated in Fig. 3 (top). The CTLE boosts the high-frequency gain by using the source-degenerated resistor (R_S) and capacitor (C_S) array to compensate for the high-frequency attenuation due to the limited bandwidth of the TIA, and the boosted AFE bandwidth can be adjusted by tuning the R_S and C_S, respectively. Since the IRN of the whole AFE circuit is mainly dictated by the relatively high gain of NFFR-TIA, the CTLE contributes negligible noise to the total IRN, thus suitable for wideband low-noise AFE design. Note that one stage CTLE only contains one peak, thus showing limited capability of bandwidth enhancement, as illustrated in Fig. 3 (bottom). Hence, two stage CTLEs are introduced, providing two peaks with two different frequencies, as shown in Fig. 3 (top left). The first stage CTLE boosts the low-frequency gain with a low-frequency peak, while the second stage's higher peak frequency further boosts the bandwidth to over-1 GHz. According to the post-layout simulation results, by properly tuning the peak frequencies of the two stage CTLEs, the bandwidth can be boosted to 1.8 GHz with a flatten in-band frequency response and an over-100 dBΩ gain.

The measured AFE AC frequency responses are present Fig. 4 (top), exhibits a 1.6-GHz bandwidth with the highest gain of 103 dBΩ, and a gain range of 73-103 dBΩ with flatten AC frequency response. The CTLE boosts the bandwidth of the AFE from 460 MHz to 1.6 GHz, as shown in Fig.4 (bottom). Fig. 5 (top) presents the measured AFE output RMS noise using an oscilloscope. The AFE is configured with 103-dBΩ gain and 1.6-GHz bandwidth. The left figure displays the combined noise of the oscilloscope and AFE, while the right figure illustrates the oscilloscope's noise. Thus, we get the integrated IRN of 109 nA and an equivalent average IRN of 2.7 pA/Hz$^{0.5}$ of our AFE accordingly. This AFE also shows low average IRN of 2-2.7 pA/Hz$^{0.5}$ within the tunable bandwidth range, as shown in Fig.5 (bottom left). Fig. 5 (bottom right) presents the 3-Gb/s output eye mask of the AFE with CTLE compensation, also demonstrating that the AFE bandwidth can be boosted to over-1 GHz. Fig. 6 depicts that our AFE achieves almost 1-order higher bandwidth of 1.6 GHz with lower average IRN, comparable gain and integrated IRN, compared to other recently published works. The 40-nm CMOS prototype occupies 0.15 mm^2 and consumes 10 mW excluding output testing buffer (OB), as shown in Fig. 7.

Acknowledgments:

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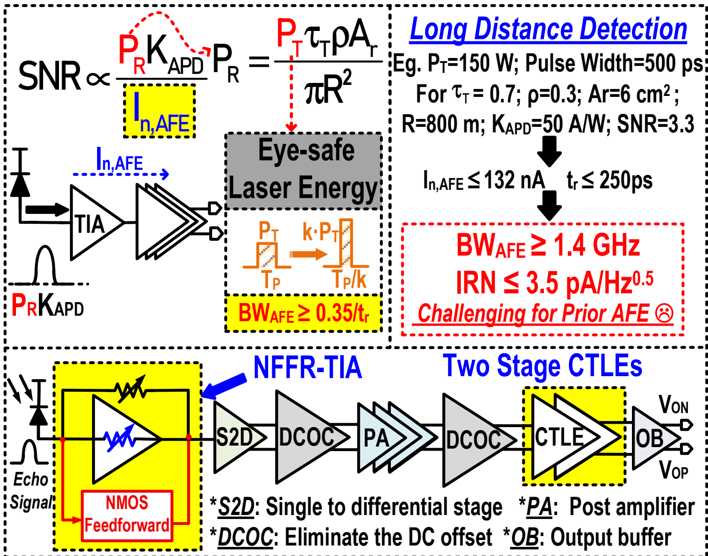


Fig. 1. Design challenges of AFE for long-distance LiDAR (top), and the proposed LiDAR AFE (bottom).

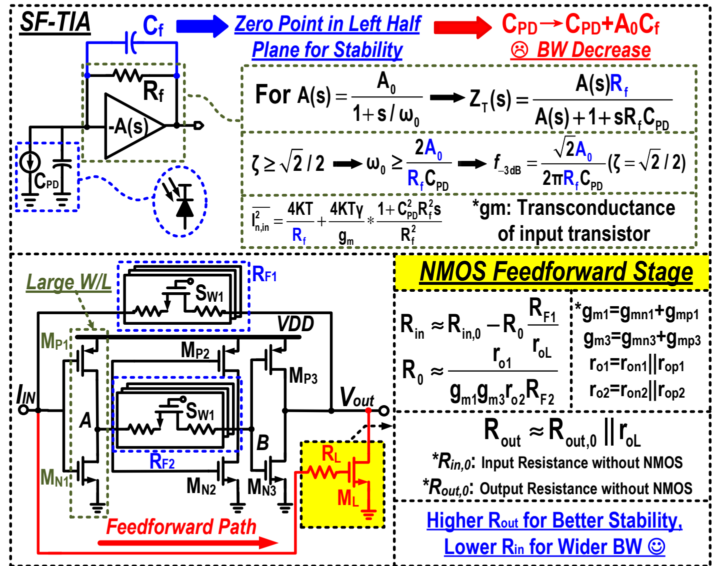


Fig. 2. Conventional capacitive compensated SF-TIA (top) and the proposed NFFR-TIA (bottom).

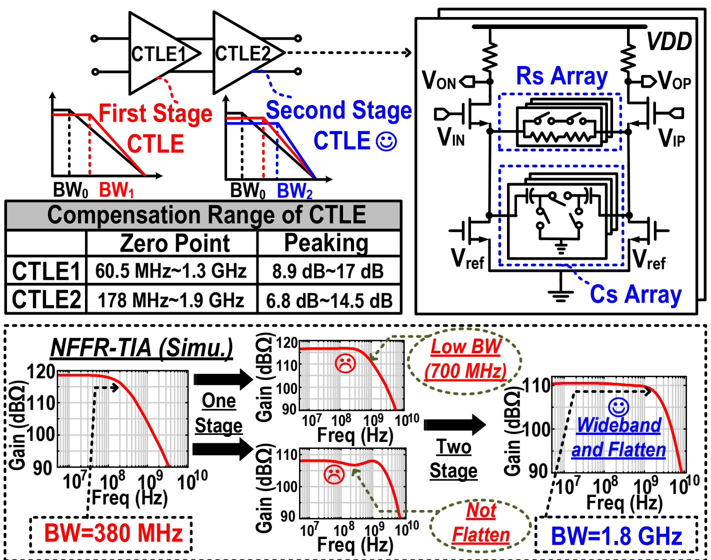


Fig. 3. Schematic (top) and simulation results (bottom) of two-stage CTLEs.

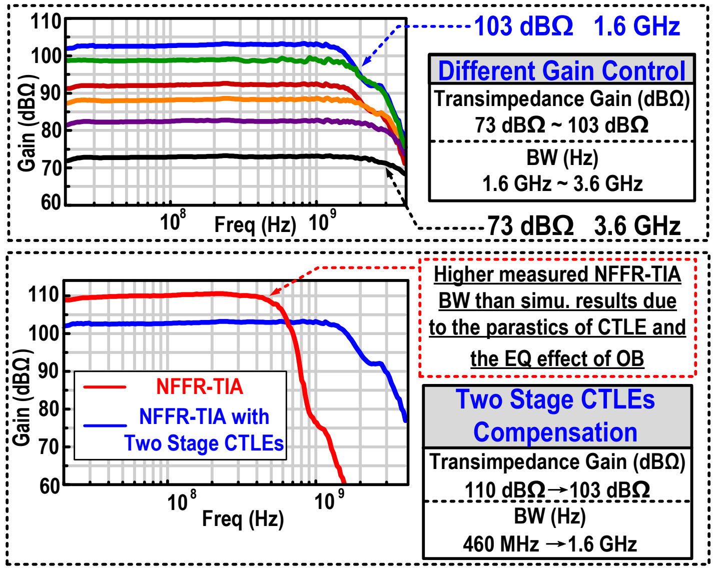


Fig. 4. Measured frequency response of AFE (top), and the measurement result of the CTLE compensation (bottom).

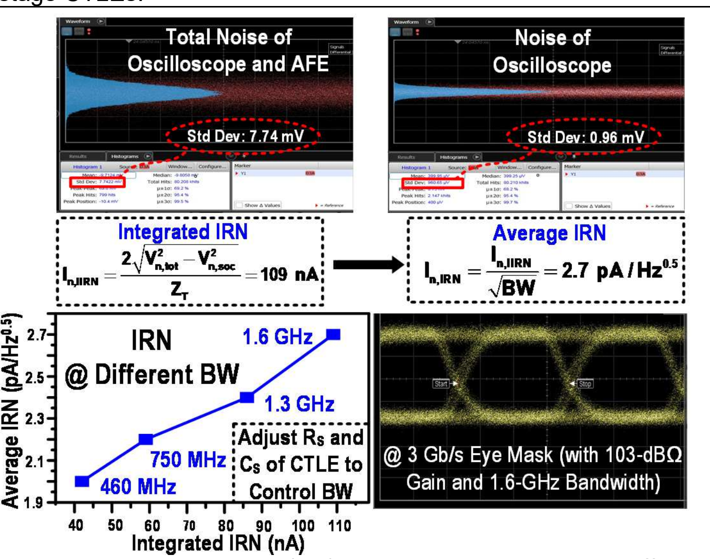


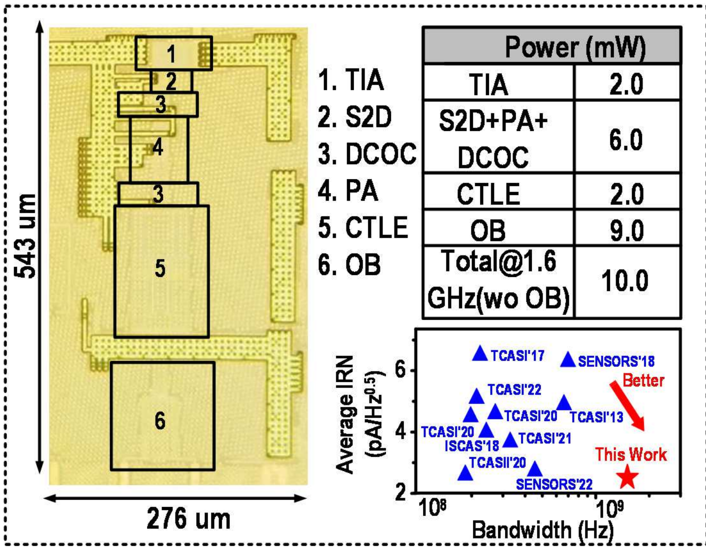
Fig. 5. Measured AFE IRN (top) at high-gain mode, IRN at different AFE bandwidths (bottom left), and output eye mask using a 3-Gb/s PRBS-31 string with CTLE compensation (bottom right).

	This work	ISSCC'20 [1]	TCASI'22 [4]	TCASI' 20 [5]	TCASI'17 [7]	TCASII'20 [6]
CMOS (nm)	40	130	65	180	350	180
Detector	APD	APD	APD	APD	APD	APD
C_{PD}(pF)	1.2	2.0	1.0	1.2	/	2
Architecture	TIA+CTLE+AMP	CURRENT AMP	TIA+AMP	TIA+AMP	TIA+AMP	TIA+AMP+EQ
Transimpedance Gain (dBΩ)	103	/	106	86	~100	101
BW (Hz)	1.6 G	200 M	220 M	281 M	230 M	190
Integrated IRN (nA)	42 (460 MHz) 109 (1.6 GHz)	70	75	78	~100	36
Average IRN ($pA/Hz^{0.5}$)	2.0 (400 MHz) 2.7 (1.6 GHz)	5.0	5.1	4.68	6.6	2.6
Power Consumption (mW)	10 (wo OB)	119 (AFE+ADC)	17 (AFE+COM)	200*	180*	37
Core Area (mm^2)	0.15	0.56	1.44**	2.2**	4**	3.41 (32 ch)

*Power consumption of the entire receiver circuit

**The area of the whole chip

Fig. 6. Performance summary and comparison.



	Power (mW)
TIA	2.0
S2D+PA+ DCOC	6.0
CTLE	2.0
OB	9.0
Total@1.6 GHz(wo OB)	10.0

Fig.7. Die micrograph, power breakdown, and performance comparisons to prior works.

Additional References:

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