A 2pA/√Hz Current-Conveyor-Assisted Ultrasound Receiver with 25pF CMUT Parasitic Capacitance

Gichan Yun[1], Kyeongwon Jeong[1], Haidam Choi[1], Seunghyeon Nam[1], Chaerin Oh[1], Hyunjoo Jenny Lee[1], Sohmyung Ha[2], and Minkyu Je[1]

[1]KAIST, Daejeon, Korea, [2]New York University Abu Dhabi, Abu Dhabi, United Arab Emirates

Ultrasound (US) imaging has emerged as a promising solution for medical diagnosis with its low cost and biocompatibility. Recent demands for multi-dimensional imaging in medical diagnosis brought a challenge of operating multiple US transducers, especially within miniaturized probes. There have been some studies of US systems for the application of intracardiac echocardiography (ICE) [1] and transesophageal echocardiography (TEE) [2] that require highly integrated systems within miniaturized probes. The miniaturization led the capacitive micromachined ultrasonic transducer (CMUT) to be a desirable choice for its compatibility with CMOS and wide bandwidth (BW) [3]. One main characteristic of the CMUT is that it generates current signals, making a transimpedance amplifier (TIA) preferable to the low noise amplifier (LNA). However, the parasitic capacitance (C_P) at the input of the TIA highly affects the performance due to the nature of converting the input-referred voltage noise at the virtual ground to the current noise by its impedance. Therefore, power consumption should be increased with a large C_P to maintain low noise. Moreover, the input multiplexer (MUX) is often used for the US imaging system to reduce overall power consumption [4]. The input switches are implemented using bulky high-voltage MOS transistors to protect the low-voltage devices of the receiver (RX) circuit from the high-voltage pulse of the transmitter (TX) circuit. It also attributes additional C_P at the input. Note that using individual transducers for TX and RX requires a larger area. Hence, the TIA should be carefully optimized for CMUT-based US imaging systems. In this work, we present an analog front-end (AFE) assisted by a current conveyor (CC) to improve noise performance while maintaining the power consumption. The CC buffers the input current and isolates the C_P of the input from the high transimpedance gain stage, relieving the overall AFE burden.

Fig. 1 shows the overall diagram of our system. We adopt a 64-channel one-dimensional (1-D) CMUT array with a C_P of 25pF. A sub-group comprises an element-level TX (8 channels) and a single AFE with an analog-to-digital converter (ADC), including an 8-to-1 MUX. The main challenge of the 1-D CMUT array is the considerable C_P due to the sizeable component size [5]. Prior works employed a resistive-feedback (RF) TIA and capacitive-feedback (CF) TIA to sense the current signal from the CMUT. The RF TIA is the most commonly used structure for its low input impedance, moderate noise figure (NF), and compact area [5–7]. However, the feedback resistor (R_F) directly adds thermal noise to the input and forms a pole with the input parasitic, which deteriorates stability and might affect the BW. It leads to a trade-off between noise and BW, which makes low-noise design challenging for large C_P. On the other hand, the CF TIA can avoid noise from the resistor by using the noiseless capacitive gain. The capacitive divider amplifies the input current while adding extra C_P to the input. Since the capacitor should be large enough to achieve the desired NF, the area can be excessive for multichannel implementation [6]. Moreover, both the input and output stages should operate with a sufficiently high bias current to satisfy the noise and BW requirements.

In the proposed RX, the CC is placed prior to the RF TIA. The CC senses the input current and transfers the amplified signal to the TIA. Although CC adds additional noise, it can significantly mitigate the requirements of the RF TIA by isolating the C_P. The simulated effective C_P of TIA in our proposed design is about 70fF, which has minimal effects on the TIA. However, the BW and noise limitations of the CC can cause problems (Fig. 2). The input impedance of the conventional CC is inversely proportional to the transconductance (g_m) of the input MOS transistors. The input impedance should be low enough since it generates a pole when combined with the input parasitic. The BW of the complete RX chain should be wide enough to process the US signal with a center frequency of 7.5MHz, which means that the g_m of the input MOS transistors should be over 1mS. One way to increase the g_m is by increasing the bias current. Since current noise increases proportionally to the bias current, unlike voltage noise, the overall input-referred noise floor would reach around hundreds of pA/√Hz to achieve the desired BW, which is too high for measuring the signal from the CMUT. To address this issue, we employ a feedback amplifier, which boosts the g_m of the input MOS transistors to use a smaller bias current, leading to low input-referred current noise. Fig. 2 plots the noise and BW performances with and without the feedback amplifier. Using the feedback amplifier, the BW of the LNA, which is the CC-assisted RF TIA, becomes about 40 times wider, and its noise is suppressed by a factor of 10 at the center frequency of the CMUT while consuming only 1.21mW.

The overall AFE design is described in Fig. 3. It consists of a CC, TIA, programmable-gain amplifier (PGA), and ADC buffer. The open-loop amplifiers used in the AFE are also shown, which are based on the current-reuse structure for low noise. The PGA and ADC buffer are implemented with the capacitively coupled instrumental amplifier (CCIA) structure. The gain of the CC is set to 6dB by manipulating the current-mirroring ratio between the input and output stages to suppress the current noise generated by the TIA. The gain of the overall RX chain can vary from 82dBΩ to 118dBΩ for time-gain compensation (TGC). It compensates for the signal attenuation caused by penetrating the tissue to relieve the dynamic range requirement of the ADC. The overall AFE achieves at least 18MHz BW for all possible gain settings, sufficient for US signal processing. The input-referred current noise of the AFE with the highest gain is 2.0pA/√Hz at 7.5MHz and 2.3pA/√Hz over BW.

The 10b SAR ADC operating at 30MS/s is adopted to digitize the analog US signal to avoid interferences or crosstalks occurring when connected to the back-end system through long wires (Fig. 4). The ADC achieves 57.6dB SNR with 1.6mW power consumption. The area and power breakdowns of the RX are depicted in Fig. 4. The total active area is 0.8452mm^2, mainly occupied by the high-voltage MUX, and the power consumption is 3.62mW, dominated by the ADC and LNA. The element-level TX with a class-D structure is also included in the chip to excite the transducer with 30V. Both the US TX and RX are fabricated in a 180nm BCD process to utilize high-voltage MOS transistors for the pulser and T/R switch. The measured TX output with a pulse width of 67ns is also shown. It can efficiently excite the transducer with a 7.5MHz center frequency.

The prototype US TX and RX ICs are verified with a single-element CMUT pulse-echo test (Fig. 5). The CMUT is placed in the oil tank, and the transmitted US signal is reflected by the quartz placed at a distance of 9mm. The CMUT is excited with a 30V pulse through the bias-tee, and the RX senses the reflected signal. The time-of-flight is expected to be 12μs considering the speed of the US in oil (c = 1460m/s). The reverberation occurs due to the reflection at the transducer, which results in signal repetitions every 12μs. Fig. 6 summarizes the proposed RX performances in comparison with other state-of-the-art CMUT-based US RX. Thanks to the proposed CC-assisted US RX, the power consumption and input-referred noise are highly reduced even for a large C_P of the CMUT. Our work achieves the best modified noise efficiency factor (NEF'), which is normalized with the C_P of the CMUT. The high-voltage TX, T/R switch, and high-speed ADC are also fabricated on chip with maintaining overall low power consumption.

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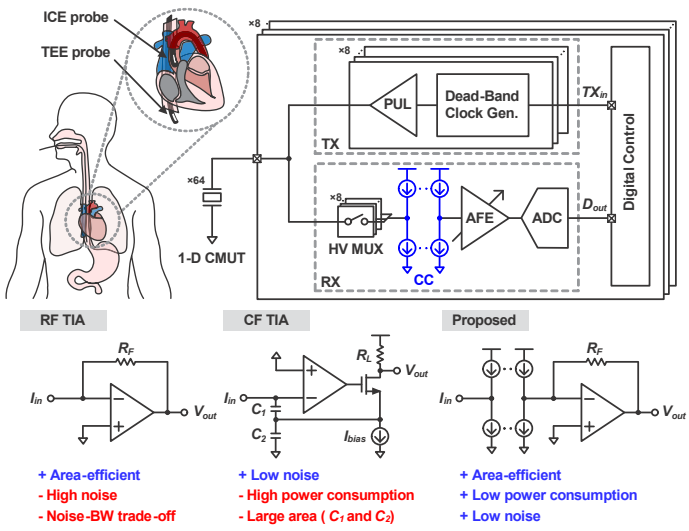

Fig. 1. Overall block diagram of the proposed US imaging system and comparison among different transimpedance stages.

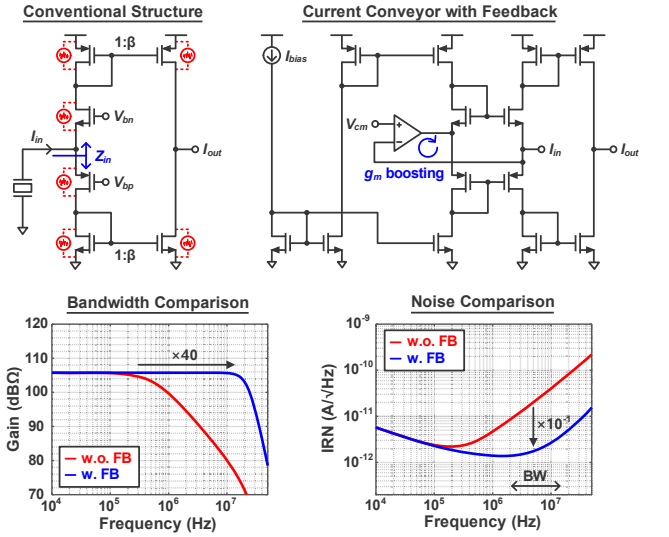

Fig. 2. Circuit diagram of the current conveyor and the comparison between the designs with and without feedback.

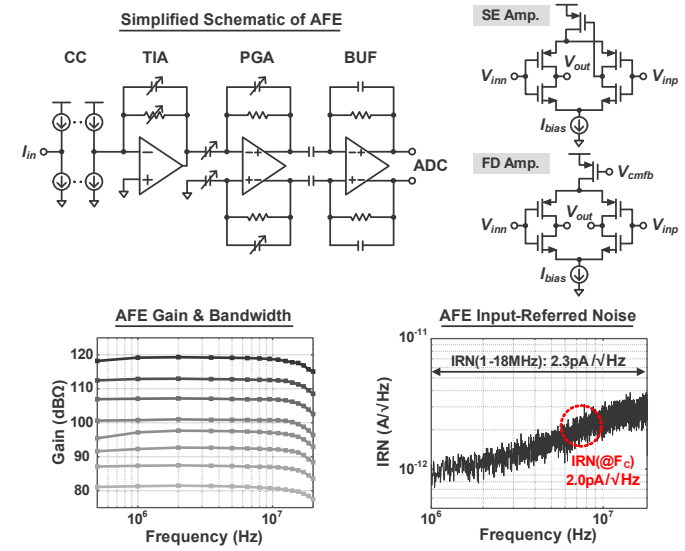

Fig. 3. Circuit diagrams and measurement results of the analog front-end.

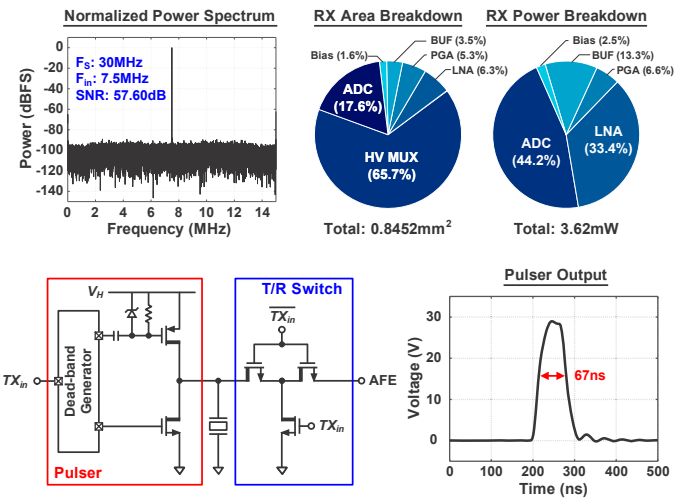

Fig. 4. Measured power spectrum and area/power breakdown of the US RX IC (top); Circuit diagram of the US TX IC and T/R switch and the output measurement result for the US TX IC (bottom).

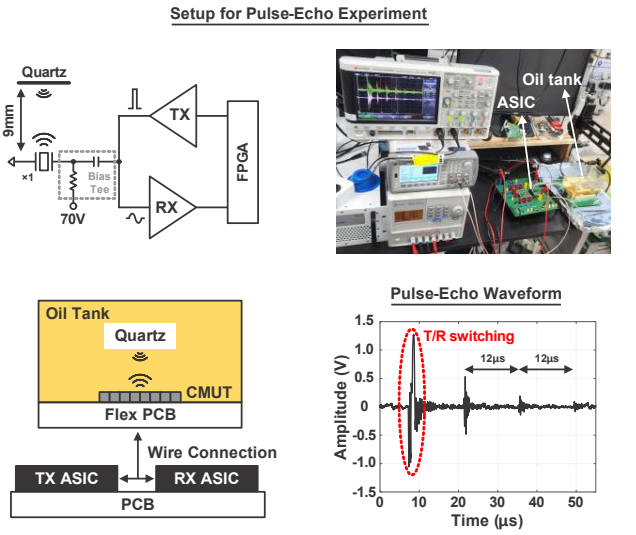

Fig. 5. Pulse-echo experiment: test setup and measured transient output waveform of the received pulse-echo signal.

	JSSC 2016 [3]	TBCAS 2017 [7]	ISSCC 2020 [1]	TBCAS 2021 [5]	This Work
Process	180nm HV CMOS	65nm CMOS	180nm HV BCDMOS	40nm CMOS	180nm HV BCDMOS
Transducer	CMUT	CMUT	CMUT	CMUT	CMUT
CMUT Cap. [pF]	2	5.5	15	25	25
Center Freq. [MHz]	5	5	5	Wideband	7.5
LNA Architecture	RF TIA	RF TIA	CF TIA	RF TIA	CC + RF TIA
LNA BW [MHz]	11	7.5	7	18	18
IRN density @F_c [pA/√Hz]	0.41 @5MHz	4.8 @2.5-7.5MHz	2.0 @5MHz	*3.1 @3-18MHz	*2.0 @7.5MHz
LNA Gain [dBΩ]	104-116	79-97	70-106	78-90	88-106
LNA Power [mW]	1.4	0.18	4.9	1.45	1.21
NEF' [pA/pF·√(mW/Hz)]	0.24	0.37	0.30	0.15	0.088
LNA Area [mm²]	<0.016	0.0035	0.12	<0.025	0.045
ADC/HV Tx on Chip	X/O	O/X	X/O	O/X	O/O
Sampling Rate [MS/s]	-	30	-	80	30
SNR [dB]	-	50.5	-	36.3	**57.6
Rx Power/Ch. [mW]	1.4	0.24	4.9	5.0	3.62

NEF': $I_{n,in}\cdot\sqrt{Power_{LNA}/C_{CMUT}}$ where $I_{n,in}$ is the input-referred current noise.
*Measured with entire AFE **Measured from ADC

Fig. 6. Performance summary and comparison.

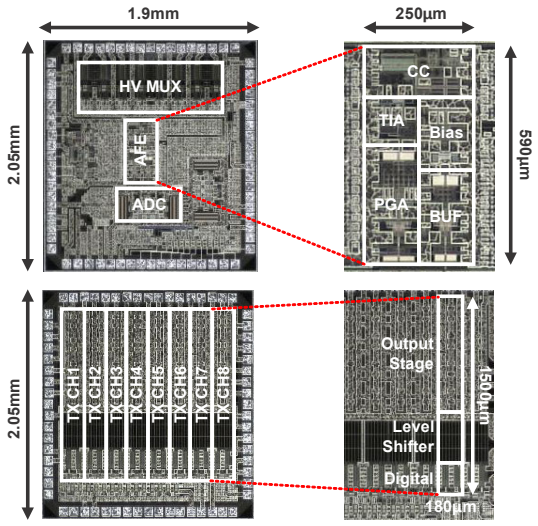

Fig. 7. Chip micrograph.

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