A 1kHz-to-62MHz 2.06zF$_{rms}$ Resolution Lock-in Amplifier with SAR-assisted Parasitic and Baseline Capacitance Compensation

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The continuous advancement of sensing technology stimulates the demand for high-precision capacitive sensor interfaces for proximity detection, material analysis, and liquid level sensing. The capacitive transimpedance amplifier (C-TIA), based on lock-in sensing principle, can extract sub-fF level capacitance changes in an extremely noisy environment with balanced resolution and speed [1,2]. However, there are still several design challenges in achieving ultra-high resolution down to zF levels. According to the equivalent capacitance noise equation in Fig.1, the parasitic capacitance C_p at virtual ground is the first factor that limits the capacitance resolution before calibration. It also reduces the bandwidth and stability of the C-TIA. The second challenge is that the dynamic capacitance of interest C_d often appears to be several orders of magnitude smaller than the inherent baseline value C_{base}, calling for a large dynamic range to accommodate both types of capacitances, which imposes stringent requirements on the SNR. Another design challenge pertains to the DC bias of the C-TIA. Conventional pseudo-resistor (PR) for DC biasing is susceptible to significant resistance variation, and can easily saturate the TIA in the case of a nA-level leakage current from the sensor [3]. Although the DC servo loop (DSL) can solve this issue, conventional PR with fixed value still imposes significant constraints on the maximum input DC current. Moreover, the PR's current noise, positively correlated to the input DC current, can dominant the C-TIA's noise performance [4,5]. Additionally, addressing the system's limitations with automatic calibration, rather than manual calibration, is crucial for increasing overall efficiency and user experience.

This work presents a precision lock-in amplifier for capacitive sensing which effectively addresses these challenges, achieving 2.06zF$_{rms}$ resolution while tolerating up to 122nA input DC current. As shown in Fig.1, the sensitivity of the proposed C-TIA is optimized via three pivotal techniques: 1) an auto-calibrated negative capacitor (NC) to nullify the parasitic capacitance C_p, such that both resolution and bandwidth of C-TIA can be improved; 2) an auto-calibrated baseline capacitance compensation which constrains the equivalent baseline capacitance to less than 5fF, enables the use of a lock-in excitation signal up to 40V$_{pp}$ to increase the SNR; 3) multi-element tunable PRs configured as R_{DC} enhance the maximum tolerance of input DC current to 122nA and provide immunity against shot noise.

Figure 2 illustrates the working principle of parasitic capacitance cancellation, which extends the NC proposed in [6] by exploiting the calibration circuit's intrinsic stability to facilitate auto-calibration. It should be noted that while an ideal NC can eliminate both noise and bandwidth degradation caused by parasitic capacitance, the actual NC implemented with active circuits introduces extra noise and high-frequency poles, which limit resolution and bandwidth respectively. However, since the requirements of the OTA inside the NC on output swing and slew rate are more relaxed than those of the main OTA, the noise contribution of the NC can be limited with relatively low power. As shown in Fig.2, the NC operates in calibration mode and sensing mode. In the calibration mode, the TIA is isolated from the NC, while the R_{DC} in the DSL is connected to V_{CM} to provide a DC bias. This feedback loop features a pole related to the calibration state. When the loop is overcompensated, this pole shifts to the right half-plane, resulting in oscillation at OTA output $V_{p,cal}$. A threshold-based oscillation detector identifies oscillations, with the subsequent logic adjusting the control words downward upon detection and upward otherwise. The threshold voltages can be reconfigured from ±30mV to ±450mV with respect to V_{CM} to ensure reliable detection of oscillation. A 9-bit SAR sequentially determines the control words. After calibrating C_p, the resolution and bandwidth of the system are enhanced by 1.33-1.85 folds and 1.15-3.85 folds, respectively (Fig.5). Moreover, in sensing mode, the NC is connected to virtual ground with near-zero signal swing, ensuring stable signal acquisition with precisely calibrated parasitic capacitance.

In this work, we employed baseline capacitance compensation (Fig.3) to further improve SNR. A 9-bit CDAC driven by inverted excitation signal is connected to the virtual ground of the C-TIA [7], acting as a negative capacitance to compensate the static baseline capacitance C_{base}. The calibration logic detects the amplitude of I-channel output after demodulation and controls the CDAC through SAR logic until $C_{b,cal} \approx C_{base}$. The CDAC is a custom-designed MOM capacitor array with an LSB of 5fF, achieving high precision and the capability of handling high input excitation voltage. After baseline compensation, the maximum amplitude of the excitation sinusoid is increased to 40V$_{pp}$, a 75-fold increase for a test capacitor of ~150fF. Note that the baseline compensation is also automatic but uses a different SAR-assisted calibration logic. This ensures that the output baseline of the I-channel (V_{out-I}) converges to V_{th}, preventing TIA saturation during signal acquisition, as illustrated by the measured baseline calibration waveforms in Fig.3.

To bias the C-TIA, this work utilizes a resistor-scaling technique [4] with a 150× current attenuator (Fig.1) to implement a large equivalent resistor and a sub-kHz low-pass corner, ensuring a low gain error at the lock-in frequency. To tolerate a wide range of input DC currents, a tunable R_{DC} is employed as illustrated in Fig.4. It consists of 16 PR units to suppress shot noise and enhance linearity [8]. The gate biasing circuit, shared by all PR units, comprises an 8-bit IDAC. This ensures an R_{DC} range of approximately 6MΩ to 1.2GΩ. The transfer functions of the C-TIA under different input DC currents are also shown in Fig.4, indicating that the C-TIA can operate with sensor leakage up to 122nA.

The prototype was fabricated in a 0.18μm CMOS process, occupying an active area of 0.84mm^2 (Fig.7). It consumes 5.3mW from a 1.8V supply. Fig.5 presents the passband and the measured output noise of the lock-in amplifier when different external capacitors (4pF-10pF) are selected to model different parasitic capacitance C_p from diverse sensors, which verifies the effectiveness of the proposed NC in terms of maximum 3.85× bandwidth extension and 1.85× noise reduction. The maximum bandwidth is 62MHz, mainly limited by on-chip and PCB parasitic capacitance of ~1pF. The bottom of Fig.5 illustrates the corresponding equivalent capacitance noise (10Hz bandwidth) of the overall system. Thanks to the proposed automatic calibration techniques, capacitance resolutions from 2.06zF$_{rms}$ to 7.86zF$_{rms}$ are achieved with different external capacitors at the input of C-TIA.

Figure 6 compares this work with state-of-the-art lock-in amplifiers. This design achieves best-in-class resolution and input DC current tolerance with highly competitive bandwidth and power consumption. Two foreground automatic calibration techniques compensate the parasitic and baseline capacitance, simplifying the sensing process at an affordable cost.

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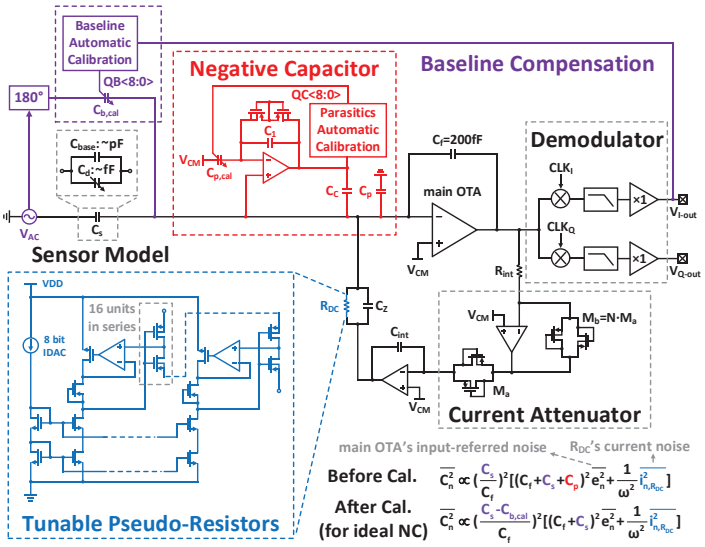

Fig. 1. Block diagram of the proposed lock-in amplifier with negative capacitor, baseline compensation and tunable pseudo-resistors.

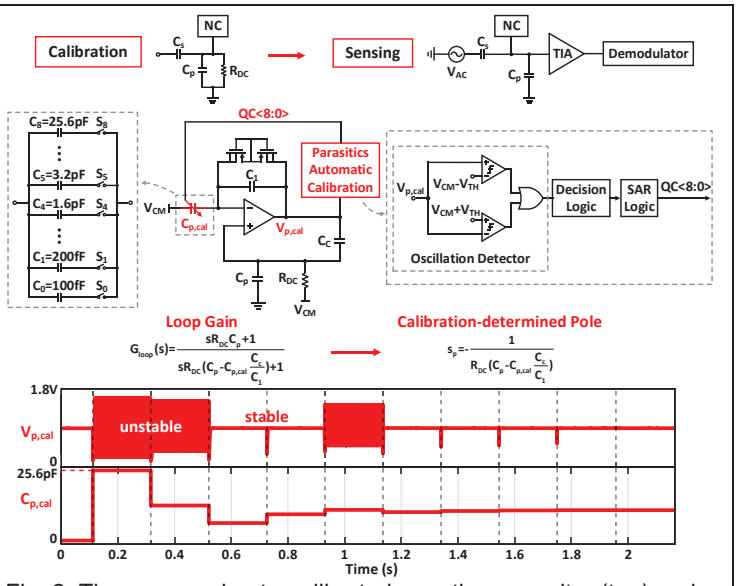

Fig. 2. The proposed auto-calibrated negative capacitor (top) and simulated convergence of $C_{p,cal}$ (bottom).

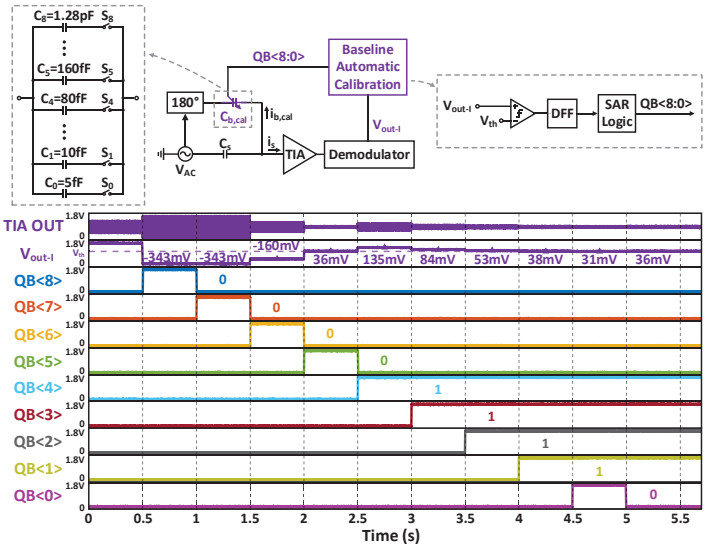

Fig. 3. The proposed automatic baseline compensation technique (top). Real-time measurement of output signals and control words during calibration (bottom).

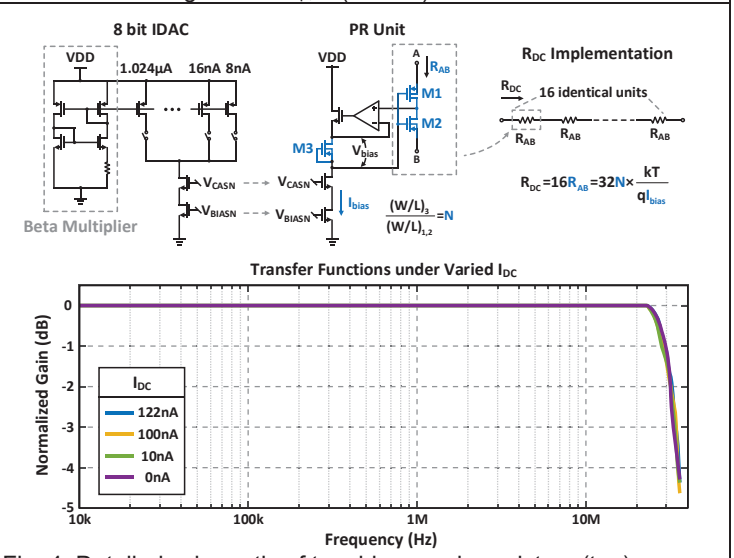

Fig. 4. Detailed schematic of tunable pseudo-resistors (top). Transfer functions of the proposed TIA under different input DC currents (bottom).

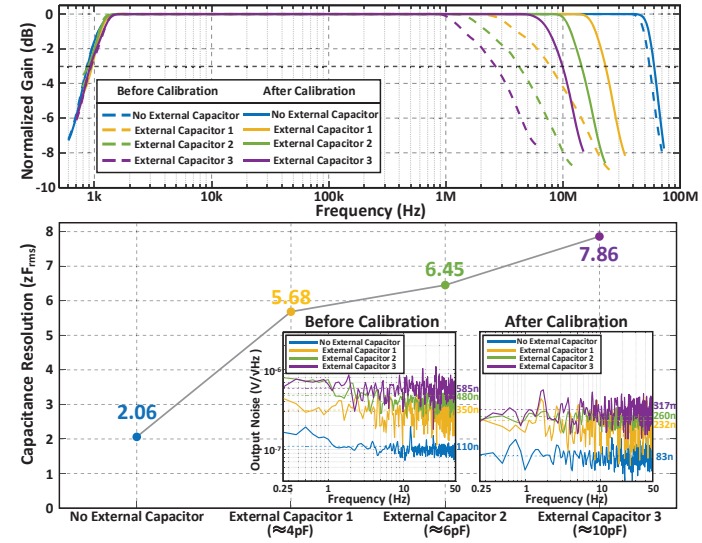

Fig. 5. Transfer function of the proposed TIA measured at different parasitic levels (top). Equivalent capacitance noise measured at different parasitic levels (bottom).

	This Work	2020 [7] SSCL	2016 [9] ISSCC	2014 [2] ISSCC	2010 [10] ISSCC	2009 [1] ISSCC
Structure	Lock-in	Lock-in	Lock-in	Mod/ Dem	Lock-in	Lock-in
Process (nm)	180	BCD 180	350	350	350	350
Supply (V)	1.8	1.8	3.3	3	3.3	3
Capacitance Resolution (rms)	2.06zF (C_p≈1pF)	*95zF	65zF	300zF	***6.4aF	1aF
Max. Input DC current (nA)	122	4	/	60	/	10
Frequency Range (Hz)	1kHz-62MHz (C_p≈1pF)	35kHz-10MHz	***DC-2MHz	1kHz - 150MHz	DC-50MHz	100Hz-2MHz
DC Bias Topology	Active	Active	Passive	Active	/	Active
Parasitics Calibration	Yes (auto)	No	No	No	No	No
Baseline Calibration	Yes (auto)	Yes (manual)	Yes (auto)	No	No	No
Power (mW)	5.3	**9	**2.63	135	**0.85	60
Active Area (mm^2)	0.84	**0.26	**0.19	1.6	1.44	0.65

*Calculated as Cap. resolution **Calculated in one channel
***Estimated from given parameters

Fig. 6. Performance summary compared with the state of the art.

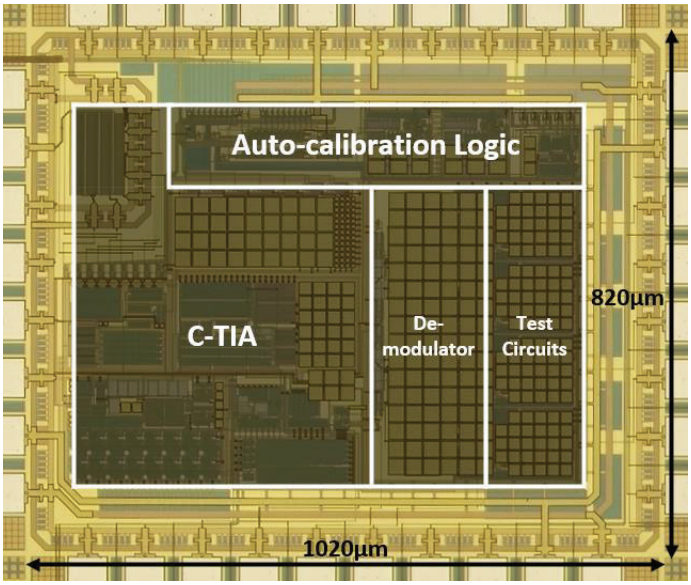

Fig. 7. Die micrograph of the proposed lock-in amplifier.

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