A 10.5 Gbps 0.55 pJ/bit PAM-3 Transceiver Using a Self-driven Dual TIA Receiver and Floating Impedance Matching for Parallel On-chip Transmission Lines

[1,3]Donghyun Yoon*, [1]Junsen He*, [2]Kwang-Hyun Baek,
[3]Youngdon Choi, [3]Junghwan Choi, and [1]Tony Tae-Hyoung Kim

[1]Nanyang Technological University, Singapore, [2]Chung-Ang University, Seoul, Korea, [3]Samsung Electronics, Hwaseong, Korea

2024 IEEE Asian Solid-State Circuits Conference (A-SSCC) | 979-8-3503-7632-6/24/$31.00 ©2024 IEEE | DOI: 10.1109/A-SSCC60305.2024.10848925

The demand for high-bandwidth and parallel interconnection for memory interfaces is steadily increasing [1]-[5]. The top of Fig.1 shows three popular structures for the memory interface. Non-return to zero (NRZ) signaling with a termination resistor has the simplest structure. However, NRZ signaling suffers from significant channel loss and power consumption due to the high clock frequency. Pulse amplitude modulation (PAM) has been proposed to extend the data rate by sending multi-bit per unit interval. However, PAM-4 consumes significant static current for intermediate levels and has a poor signal-to-noise ratio (SNR). Thus, complicated equalizing techniques are employed, leading to significant power consumption. However, PAM-3 offers a higher SNR, and removes the reference voltage (V_{REF}) using inverter-based TIA, which makes PAM-3 transceivers more area- and power-efficient than PAM-4. However, the large static current at the Mid-level is still the fundamental limitation of PAM-3. Therefore, this paper proposes the self-driven receiver (SDR) to remove the static current in the PAM-3 transmitter (Tx) by deactivating it. The floating impedance matching (FIM) for the Mid-level reduces the channel reflections at the deactivated Tx. Finally, the dual TIAs in SDR improve signal integrity by separating the top and bottom eyes, and reduce power consumption by employing biased inverters.

The bottom of Fig. 1 shows the top block diagram of the proposed PAM-3 transceiver for on-chip transmission lines or die-to-die interconnection. In the Tx, the pattern generator provides the NRZ pseudo-random bit stream (PRBS) 7 pattern. The NRZ data is encoded to PAM-3, and feed-forward equalizer (FFE) logic generates the signals to drive the main driver, Mid-level equalizer (M EQ.), and High/Low-level equalizer (H/L EQ.). The main driver is turned off for the Mid-level output, and the receiver (Rx) input is self-driven by the dual TIAs. The FIM network provides impedance matching at high frequencies without static current. The PMOS-enhanced (PE) and NMOS-enhanced (NE) TIAs separate the Rx input eye using different threshold voltages to enhance each eye height and reduce power consumption. The upper eye is amplified by the PMOS-enhanced TIA, and the bottom eye is vice versa.

In the conventional PAM-3 transmitter, the PMOS and NMOS are turned on together to generate the Mid-level voltage, which consumes significant static current ($I_{static,M}$). To tackle this issue, this work proposes an SDR to generate the Mid-level voltage by itself. Therefore, the Tx can be turned off for the Mid-level, which reduces power consumption. As shown in the PAM-3 truth table in Fig. 2, the Mid-level occupies 37.5% of PAM-3 data. Since $I_{static,M}$ is half of the static current of the High-level ($I_{static,H}$), the proposed SDR reduces the main driver power by 42.3% and the total Tx power, including peripheral circuits, by 13.5%, as shown in the bottom-right of Fig. 2. However, the deactivated Tx has infinite output impedance and creates signal reflections due to impedance mismatches. This work proposes FIM for tackling the impedance mismatch issue. The FIM network consists of a series connection of resistor and capacitor, modeled as "$1/sC_T+R_T$". The equivalent impedance approaches R_T at high frequency. The larger C_T generates the lower reflection (S_{11}), as depicted at the bottom of Fig. 2. The best S_{11} is -15.7 dB with a C_T of 1pF. However, the 0.1 pF is selected in this work after considering the area efficiency. The proposed FIM offers a 2.8 dB improvement with 0.1 pF. The FIM network is connected to the Tx output only when transmitting the Mid-level. Thus, it does not increase capacitance for the High- and Low-levels. C_T is not critical for the Mid-level at the Rx since the Rx input is driven by itself.

The inverter-based TIA has a simple structure for PAM-3 signaling without V_{REF}. However, the signal amplitude is limited by the supply voltage, as shown at the top of Fig. 3. Thus, the maximum theoretical eye height is 0.5 VDD. In addition, TIA consumes a large static current when the TIA input and output are 0.5 VDD. This work proposes the dual TIA using two different threshold voltages to enhance the eye height and reduce power consumption. The proposed dual TIA, shown at the bottom of Fig. 3, generates the top and bottom eyes separately. The PMOS-enhanced TIA (PE TIA) comprises a strong PMOS and a weak NMOS to amplify the top eye. It has a threshold of $V_{TH,H}$, which is the center of the top eye. The NMOS-enhanced TIA (NE TIA) is vice versa. The DC characteristic curve shows that the dual TIA output voltages are close to the VSS and VDD for 0.5 V input, reducing the amount of static current for the Mid-level input compared to the prior single TIA. Even though two TIAs are used in the proposed dual TIA, the peak current flowing through the dual TIA is only 65 % of the single TIA, as shown in the bottom-right of Fig.3. However, the weak NMOS transistor in PE TIA limits the slew-rate of falling edge (especially for High/Mid-level to low-level in TIA_H) and degrades the SNR (the eye diagram of TIA_H in Fig. 3). The weak PMOS in NE TIA is vice versa. The feedback resistance is doubled in the dual TIA to keep the overall equivalent impedance.

The proposed PAM-3 driver's schematic and control logic are depicted in Fig. 4. The addition-only FFE is adopted to reduce power consumption. For example, if the previous bit is Mid- or High-level, N_{EQ} is activated. The FFE control logic is implemented with a half-to-full rate converter to reduce the clock frequency. In addition, the fractional FFE is used for Mid-level equalization to improve eye width. The bottom-left of Fig.4 shows the eye diagram of the conventional and fractional FFE for the Mid-level. Because the fractional FFE is disabled after reaching the target Mid-level, it offers a wider eye width. However, the short pulse has been required to implement the fractional FFE. On the other hand, the M EQ. tap is implemented using a stacked MOS structure in this work. The delay between the M/MB and MN_{EQ}/MP_{EQ} generates fractional equalization without a short pulse. The delay is controlled by a digitally controlled delay line (DCDL).

The proposed PAM-3 transceiver and on-chip channels are fabricated in a 65 nm CMOS process. Fig. 7 illustrates the chip die photo. The top-left of Fig. 5 shows the on-chip channel schematic and characteristics. The 3 dB bandwidth and channel loss at 5.25 GHz are set to 2.13 GHz and -8.71 dB, respectively. The top-right of Fig. 5 presents the measured bit error ratio (BER) bathtub curve of the center channel, which has the largest crosstalk. At 10.5 Gbps, the proposed transceiver shows the 0.36 UI with crosstalk. If the other five channels are disabled, the eye width increases to 0.43 UI. The BER over the comparator reference voltage (V_{COMPH} and V_{COMPL}) offset is shown in the bottom-left of Fig. 5. Also, the BERs with and without FFE are compared at 6 Gbps, as shown in the bottom-right of Fig. 5. In the top of Fig. 6, the eye diagram of TIA outputs are measured at 10.5 Gbps using the TIA monitoring block in the bottom of Fig. 1. The PE and NE TIA output's eye heights are 211 mV and 288 mV, respectively. The performances of recent PAM-3 and NRZ transceivers with on-chip channels are compared at the bottom of Fig. 6. Because the proposed SDR and dual TIA reduce the static current of Mid-level, the proposed transceiver achieves the best energy efficiency of 0.55 pJ/bit among the PAM-3 transceivers. Even though the work in [5] shows slightly lower energy, it requires additional supply voltage for the Mid-level, and the power for generating the additional supply voltage was not considered in the measurement. The active area and power consumption of the proposed transceiver per channel are 0.00381 mm^2 and 5.775 mW, respectively.

Acknowledgement: This work was supported by Ministry of Education, Singapore, under AcRF Tier-1 (RG136/23).

References:

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[3] P. -W. Chiu et al, "A 65-nm 10-Gb/s 10-mm On-Chip Serial Link Featuring a Digital-Intensive Time-Based Decision Feedback Equalizer," JSSC 2018, pp. 1203-1213.

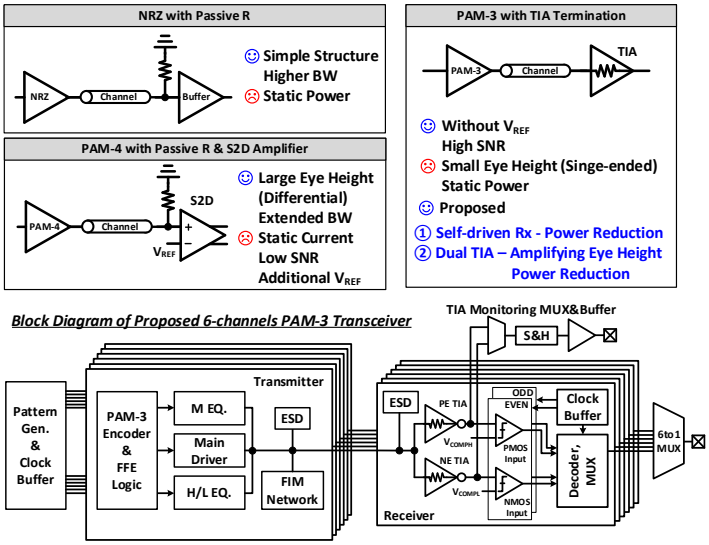


Fig. 1. Memory interface architectures and block diagram of the proposed PAM-3 transceiver.

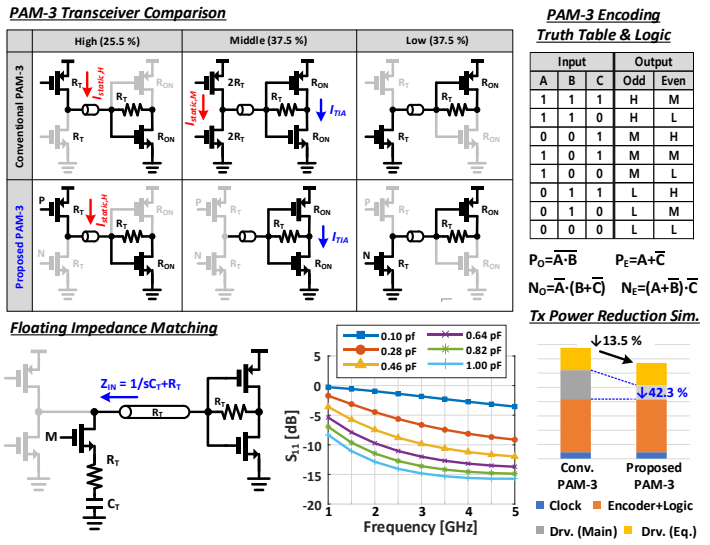


Fig. 2. Operation of the proposed PAM-3 transceiver and floating impedance matching.

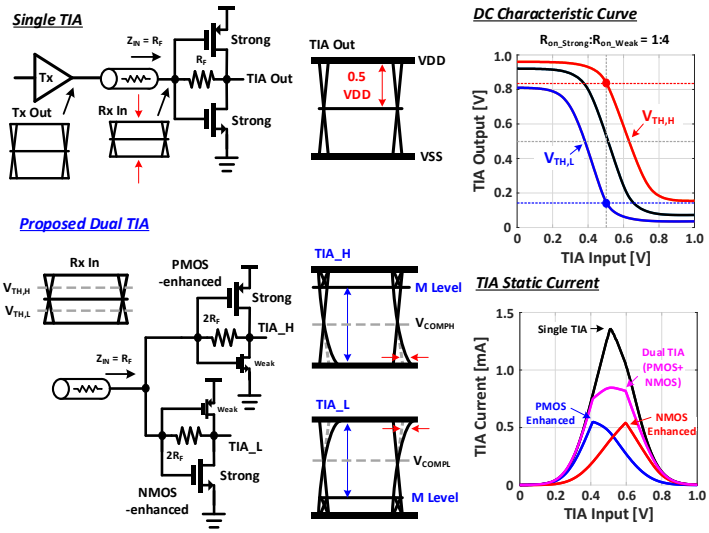


Fig. 3. Single TIA and the proposed dual TIA with enhanced eye diagram.

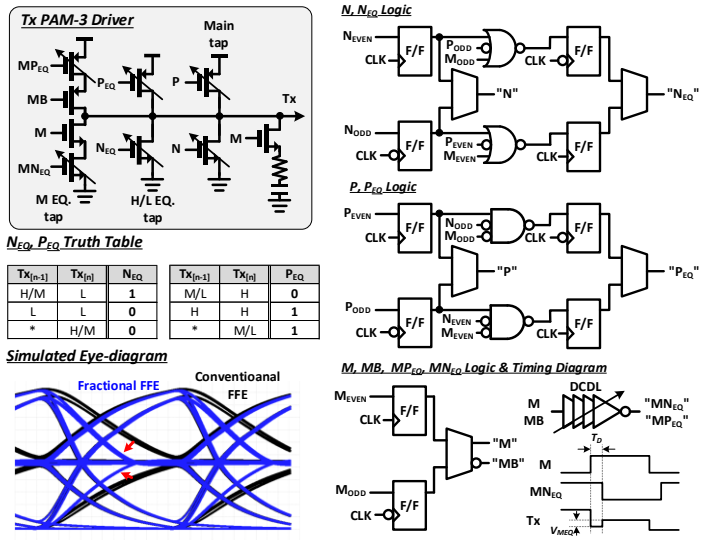


Fig. 4. PAM-3 driver schematic and control logic.

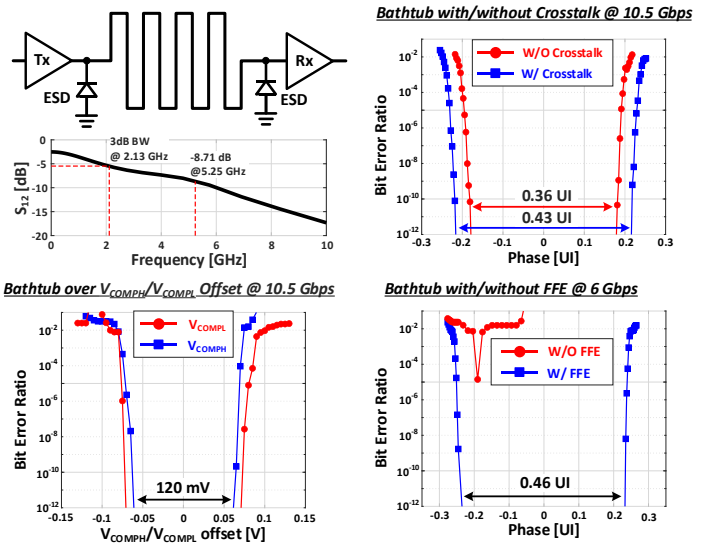
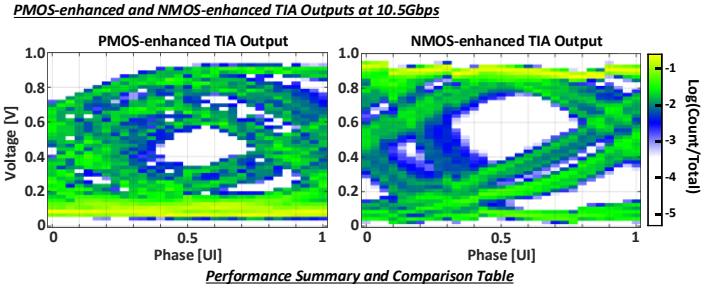


Fig. 5. On-chip channel characteristics and measurement results.



Performance Summary and Comparison Table

	JSSC18 [3]	ISSCC20 [4]	ISSCC22 [5]	JSSC21 [1]	JSSC23 [2]	This work
Process [nm]	65	65	28	28	28	65
Data Rate [Gbps]	10	4	10	30	33	10.5
Termination	Inverter-based TIA	RGC-TIA	Inverter-based TIA	S2D Amp. with Passive R	S2D Amp. with Passive R	Inverter-based TIA
Signaling	NRZ	NRZ	NRZ (Di-code)	PAM-3	PAM-3	PAM-3
Number of Channel	1	6	8	1	1	6
Channel Length [mm]	10	6	[$] 6	80	20	[$] 5
Energy Efficiency [pJ/bit]	0.772	1.524	[#] 0.35	1.11	1.09	0.55
Eye Width [UI]	0.43	0.74/0.4	0.47	0.14	-	0.36
Area/Channel [mm^2]	0.00232	0.01995	0.00460	0.01400	0.00600	0.00381

[$] with ESD diode (Higher channel loss) [#] Additional supply for Mid-level (Not including power for additional supply)

Fig. 6. Measured TIA output eye diagram and performance comparison table.

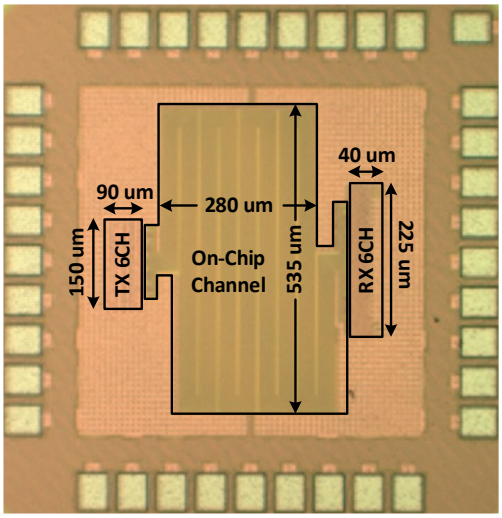


Fig. 7. Die micrograph.

Additional References:

[4] H. -G. Ko et al, "An 8Gb/s/μm FFE-Combined Crosstalk-Cancellation Scheme for HBM on Silicon Interposer with 3D-Staggered Channels," ISSCC 2020, pp. 128-130.

[5] H. Park *et al*, "A 0.385-pJ/bit 10-Gb/s TIA-Terminated Di-Code Transceiver with Edge-Delayed Equalization, ECC, and Mismatch Calibration for HBM Interfaces," ISSCC 2022, pp. 1-3.