A 118.89 Tb/s/mm/pJ/bit 18-Gb/s/wire Run-Length-Tolerant Transition-Driven AC-Coupled Transceiver for Short-Reach Die-to-Die Interfaces

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Multiple process designs are integrated into a single package in recent Chiplet configurations, where die-to-die interfaces employ multi-lane configuration for high data bandwidth, requiring small-area low-power transceivers (TRXs). Aggressively lowering the TX V_{DDQ} reduces power consumption, and the low-swing transmitted data can be sampled using a PMOS-based sampler [1], [2] or a transimpedance amplifier (TIA) [3] in the RX. However, the sampling performance of the PMOS-based sampler is poor, and a large-area voltage reference generator (VrefGen) is needed (Fig. 1 top left). The VrefGen can be shared with multiple RX to reduce area, but the device mismatch between lanes causes the offset problem. The TIA-based RX omits the VrefGen, but the static or short current of the TIA increases the power consumption (Fig. 1 bottom left). Although capacitive driving [4] reduces the current consumption, the run length limitation or the large-size capacitor should be required to prevent baseline wander problems (Fig. 1 top right). To solve these problems, we propose a transition-driven TRX for low-area and low-power die-to-die interfaces (Fig. 1 bottom right). Key contributions are as follows: 1) an AC-coupled capacitor is incorporated in the RX front end, and only the transition information is received; 2) a low DC level of the received data (D_{RX}) is recovered using a PMOS holder, and a high DC level of D_{RX} is recovered using a feedback-based NMOS holder. Through this method, a small-size AC capacitor can be used without run-length limitation; 3) By setting ($D_{RX,H}$+$D_{RX,L}$)/2 level around the trip point of the inverter, a simple inverter-based RX can be implemented. Furthermore, TX V_{DDQ} can be aggressively lowered owing to the inherently level-shifting characteristics of the proposed RX.

Fig. 2 shows the operation of the proposed transition-driven TRX under two transition cases. During the low-to-high transition, the TX pull-up (PU) driver is turned on, driving RX_IN from 0 V to V_{DDQ} through the on-chip channel. The coupling capacitor C_{TRAN} transfers only the rising transition information from RX_IN to BUF_IN by $\Delta V_{RX\_IN} \cdot C_{TRAN}/(C_{TRAN}+C_{PAR})$, where C_{PAR} represents the parasitic capacitance at the BUF_IN node. When V_{BUF_IN} exceeds the inverter trip-point voltage (V_{TRIP}), the inverter's high gain enables a rapid transition of V_{BUF_OUT} from 0 V to V_{DD}. After this transition, the output of the RX (BUF_OUT) is fed back to turn on NMOS holder N2, and a small NMOS bias current (I_{HIGH}) through transistors N1 and N2 provides a small DC current path from V_{DD} to V_{DDQ}, holding V_{BUF_IN} above V_{TRIP} and maintaining the high state with negligible static power consumption. This bias path ensures robust maintenance of the high-level state regardless of run-length. Conversely, in the high-to-low transition, the pull-down (PD) driver is activated while the PU is disabled, returning V_{RX_IN} to 0 V. A transient swing of equal magnitude and opposite polarity, relative to the low-to-high transition, is capacitively coupled to BUF_IN. When V_{BUF_IN} falls below V_{TRIP}, V_{BUF_OUT} transitions from V_{DD} back to 0 V. During consecutive '0' inputs, PMOS holder P1 remains active with its gate at 0 V, holding V_{BUF_IN} at V_{DDQ} regardless of run-length.

Fig. 3 (top) compares DC wander in an AC-coupled RX and the proposed RX. The proposed RX uses PMOS/NMOS holders to suppress DC wander, enabling a compact 130-fF coupling capacitor well suited for area-constrained die-to-die interfaces. When the same 130-fF coupling capacitor is used in the AC-coupled RX, the eye margin degrades due to DC wander. Fig. 3 (bottom left) shows the coupling-capacitive feed-through during the high-to-low transition causes an undershoot below V_{DDQ}, thereby reducing the vertical eye margin. To address this, we employ a compensation capacitor (C_{COMP}) to generate compensation current (I_{COMP}) for mitigating the undershoot. Fig. 3 (bottom right) shows the flow of the TX pull-down current ($I_{TX,\,PD}$) and I_{COMP}. C_{COMP} increases the duration of I_{COMP} flow by the amount of time that N2 momentarily turns on for the buffer delay time (t_d), thereby improving eye margin.

Fig. 4 (top) shows the top-level block diagram of the proposed transceiver, comprising three TX and three RX interconnected through high-density on-chip channels replicating a silicon interposer. The TX of each lane has a 64-b pattern generator, which produces a PRBS pattern or a continuous '0' pattern. 64-b parallel data are transmitted to the 64:2 SER; its true and complement outputs are transmitted to the N-over-N output driver through 2:1 SER. The N-over-N output driver transmits low-swing signals to the RX through a programmable on-chip channel; the proposed RX then restores them to full-swing CMOS levels based on voltage transitions. BUF_{OUT} is sent to an external bit-error-rate tester (BERT) through 1:8 DESER and a pseudo-open-drain (POD) driver to be analyzed. Fig. 4 (bottom) shows the programmable three-lane 2-μm pitch on-chip channel implementation and frequency response for various insertion loss and far-end crosstalk (FEXT) conditions. A digitally controlled metal-oxide-metal capacitor array is connected beneath each channel, adjusting channel loss.

The prototype chip, including the proposed die-to-die interfaces, was fabricated in a 28-nm CMOS process. Fig. 5 (top) shows the measured BER bathtub curves at 12.5 Gb/s without aggressor signals, where CH1 transmits three PRBS patterns while CH0 and CH2 are held at continuous zeros. The channel loss was adjusted using different CapBank[5:0] settings. As the CapBank code increases from 6'b000000 to 6'b101010, the horizontal eye opening gradually degrades due to increased insertion loss. Fig. 5 (bottom left) shows the horizontal eye opening of CH1 when CH0 and CH2 operate as aggressors at a data rate of 12.5 Gb/s. When the CapBank code is set to 6'b000000 (minimum channel loss), the link operates up to 18 Gb/s; Fig. 5 (bottom right) shows the horizontal eye opening at this rate. The PRBS-31 pattern verification shows the proposed RX is immune to long run-length.

Fig. 6 (top) presents the performance comparison with recently reported die-to-die interfaces. In the RX, this work reuses the driver voltage V_{DDQ} used for reducing TX power, enabling a simplified RX design using only an inverter-based buffer, a capacitor, and a few transistors. Therefore, the proposed TRX is well suited for die-to-die interfaces that demand both low power and minimal area. Fig. 6 (bottom) shows a five-layer interposer model used to calculate the effective edge bandwidth [5].

Fig. 7 shows the die micrograph of the prototype TRXs and programmable on-chip channels and the power breakdown.

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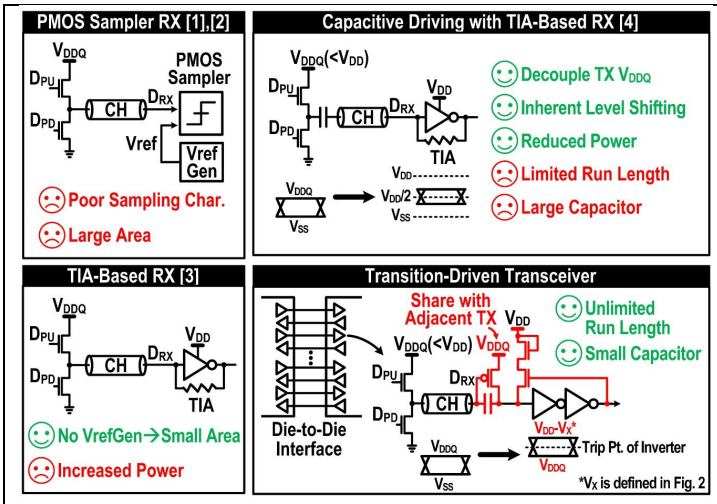


Fig. 1: Prior PMOS sampler-based RX (top left), TIA-based RX (bottom left), capacitive driving with TIA-based RX (top right), and proposed transition-driven transceiver (bottom right).

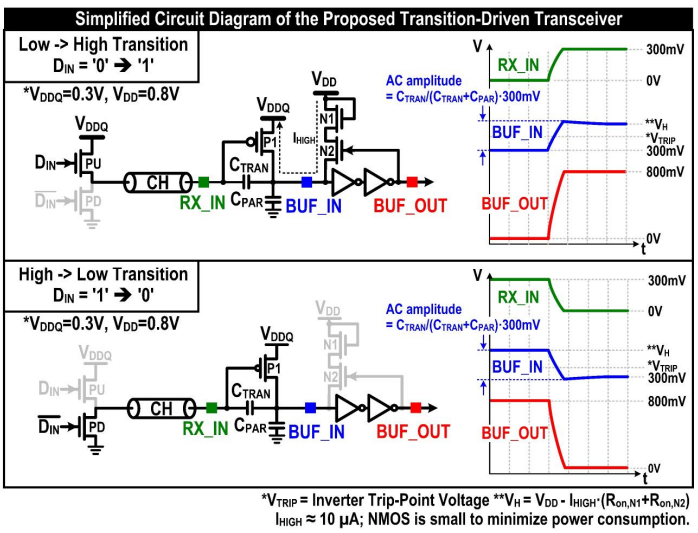


Fig. 2: Operation of the proposed transition-driven transceiver, showing low-to-high (top) and high-to-low transition (bottom).

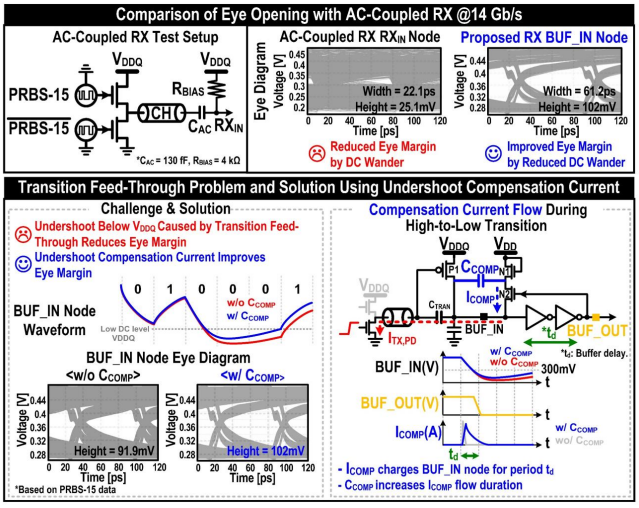


Fig. 3: Comparison of DC wander characteristics in ac-coupled RX and transition-driven RX (top) and detailed challenge and solution in implementing transition-driven RX (bottom).

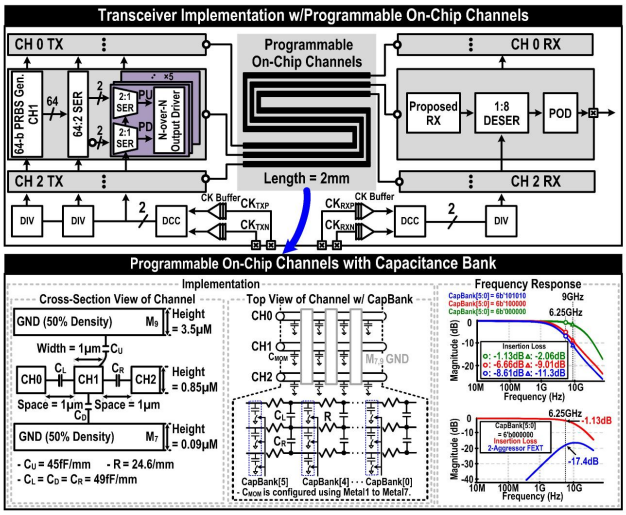


Fig. 4: Circuit implementation of the proposed die-to-die interface (top) and detailed on-chip channel implementation and frequency response (bottom).

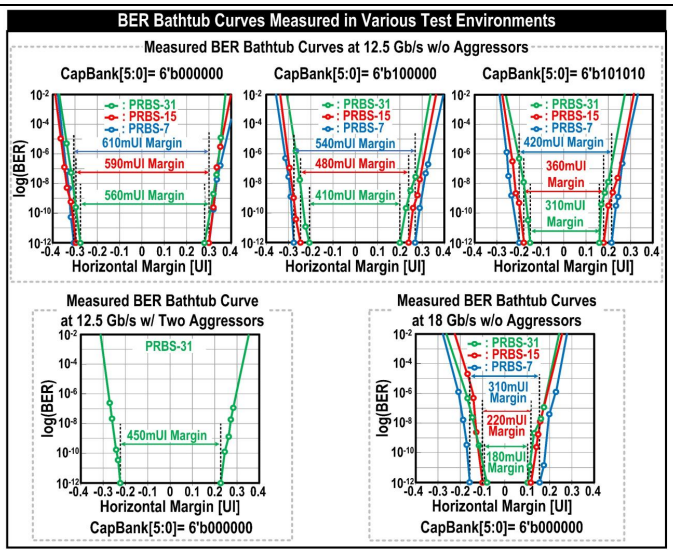
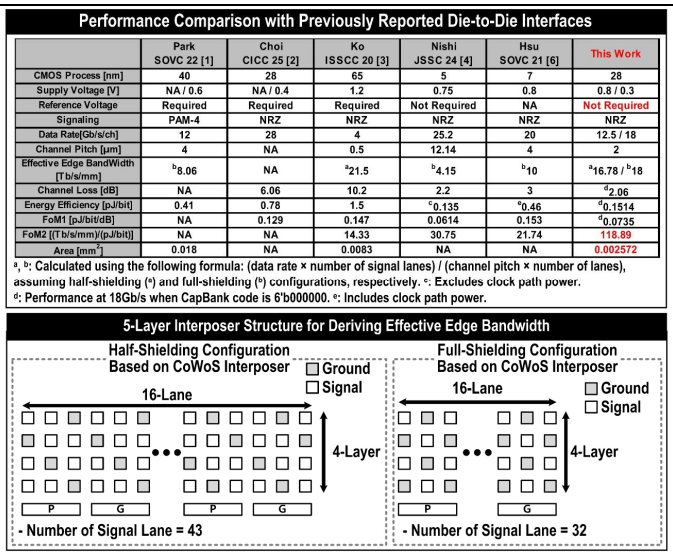


Fig. 5: BER bathtub curves measured in various test environments.



	Park SOVC 22 [1]	Choi CICC 25 [2]	Ko ISSCC 20 [3]	Nishi JSSC 24 [4]	Hsu SOVC 21 [6]	This Work
CMOS Process [nm]	40	28	65	5	7	28
Supply Voltage [V]	NA / 0.6	NA / 0.4	1.2	0.75	0.8	0.8 / 0.3
Reference Voltage	Required	Required	Required	Not Required	NA	Not Required
Signaling	PAM-4	NRZ	NRZ	NRZ	NRZ	NRZ
Data Rate[Gb/s/ch]	12	28	4	25.2	20	12.5 / 18
Channel Pitch [μm]	4	NA	0.5	12.14	4	2
Effective Edge BandWidth [Tb/s/mm]	[b]8.06	NA	[a]21.5	[b]4.15	[b]10	[a]16.78 / [b]18
Channel Loss [dB]	NA	6.06	10.2	2.2	3	[d]2.06
Energy Efficiency [pJ/bit]	0.41	0.78	1.5	[c]0.135	[e]0.46	[d]0.1514
FoM1 [pJ/bit/dB]	NA	0.129	0.147	0.0614	0.153	[d]0.0735
FoM2 [(Tb/s/mm)/(pJ/bit)]	NA	NA	14.33	30.75	21.74	118.89
Area [mm²]	0.018	NA	0.0083	NA	NA	0.002572

[a], [b]: Calculated using the following formula: (data rate × number of signal lanes) / (channel pitch × number of lanes), assuming half-shielding ([a]) and full-shielding ([b]) configurations, respectively. [c]: Excludes clock path power. [d]: Performance at 18Gb/s when CapBank code is 6'b000000. [e]: Includes clock path power.

Fig. 6: Performance comparison table (top) and 5-layer interposer model for calculating effective edge bandwidth (bottom).

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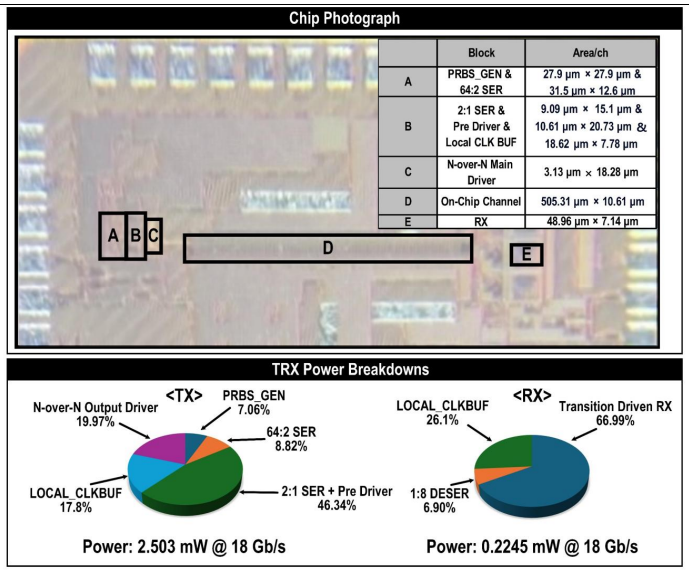

Fig. 7: Chip photograph of the prototype chip and power breakdown.

Additional References:

[5] Y. -J. Huang et al., "UCIe-compliant chiplet interconnect design leveraging cutting-edge packaging technologies," IEEE CICC, Apr. 2025, pp. 1–8.

[6] Y. -Y. Hsu et al., "A 7nm 0.46pJ/bit 20Gbps with BER 1E-25 die-to-die link using minimum intrinsic auto alignment and noise-immunity encode," IEEE SOVC, June 2021, pp. 1–2.

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