A CMOS Low-Noise Fast-Settling BM-TIA with CM-Post-Amplifier Chip Connectivity for 50G-PON

Yifei Xia, Zhixing Zhang, Shuaizhe Ma, Yuanhao Yao, Ruixuan Yang, Yuye Yang, Jianyu Yang, Li Geng, Dan Li, Email: dan.li@xjtu.edu.cn

Xi'an Jiaotong University, Xi'an, China

With the bandwidth demand keeps growing, the next generation 50Gb/s Passive Optical Network (PON) is on the horizon. As the high-speed access network for most users, the increase in the cost of devices and modules makes low-cost components more desirable. Meanwhile, the multi-Km transmission distance and several layers of lossy optical splitter in PON dictate more sensitive receiver than those used in the datacenter. In the optical line termination (OLT) side, high-speed burst-mode (BM) transimpedance amplifiers (TIA) are mostly made by SiGe BiCMOS [1-3] to realize the harsh noise and settling time targets, with higher cost and large power consumption. Targeting on datacenter applications, some recent CMOS TIAs [4-5] have accomplished rapid BM settling through mixed-signal techniques. However, they can't be easily applied to BM-TIA for PON in the absence of clocking. Moreover, the post-amplifier chip that follows the BM-TIA needs also to be burst-mode amplifier, further complicating the system design with deteriorated performance and cost. In this paper, we address the noise and settling time challenges in the design of a 50-Gb/s CMOS BM-TIA for low cost, which also highlights its unique capability to drive a continuous-mode (CM) post-amplifier chip in BM application.

Figure 1 describes the architecture of the BM-TIA and its design approach. The RF signal path includes the front-end (FE) TIA, the single-to-differential amplifier (S2D), two continuous time linear equalizers (CTLEs), the residual offset canceller (ROC), the pre-driver and the output buffer. BM automatic offset cancelation (AOC) and AGC are merged in one block. Starting from the simple one-stage feedback TIA with a commonly applied the feedback resistor (R_F) value of 350Ω [6-7], the TIA bandwidth and its input-referred noise density (IRND) are 7.5GHz and 16 pA/√Hz, respectively. Then the R_F is scaled up [10] to 1.4kΩ to reduce the low-frequency noise floor from 12.6 pA/√Hz to 5.3pA/√Hz, but the TIA bandwidth in this case shrink to only 1.3GHz due to lack of gain in the core amplifier. Therefore, a three-stage amplifier is used [11] to provide sufficient forward gain to restore the TIA bandwidth back to 8GHz, along with the help a feedback capacitor C_F in parallel with R_F to recover the TIA loop phase margin from 30° to 67°. Since this high-order TIA introduces more high-frequency gain roll-off than the typical one-stage TIA, a pair of on-chip inductors L1 and L2 is introduced to the FE-TIA. Shown in Fig. 1(e), not only the bandwidth of the FE-TIA is raised to 11.5GHz, but also the undesirable high-Q serial peaking from the photodiode (PD) capacitance and the input bondwire inductance at 32GHz is suppressed and spitted, forming a smoother in-band gain roll-off of the FE-TIA to ease the design of the following equalization stages. The peaking split also suppresses the TIA noise in the 10GHz-30GHz and 35GHz+ frequency bands. Finally, the CTLEs form a broadband peaking centered at 28GHz to reach an optimum frequency response, resulting a total bandwidth of 28GHz and IRND of 7.8pA/√Hz for the signal path. Compared with the initial simple TIA, the bandwidth is extended by roughly 4× while the IRND is reduced by more than 2×. In addition, the TIA also incorporates low-gain mode for large input current, where R_F and forward gain are reduced in sync for stability.

Figure 2(a) details the proposed fast AOC and AGC topology, including a variable time constant analog feedback loop and its control logic (CTRL). Since the analog loop can't be made fast enough under reasonable offset cancellation accuracy [12], various loop speed-up methods are devised, depicted in Fig. 2(b). In the first AOC phase, once the loop is turned on with a sufficient input current level, after an initial one-step charge pumping to raise V_G to one V_{TH} of the transistor, a large current of 800μA is injected to V_G node for fast charging until it's called off by CTRL. The second AOC phase is relatively short given the fact that the loop has entered its quick small-signal settling state, which is sped up by a factor of the loop gain over its large-signal time constant set by the open-loop main pole. In the meantime, gain control is executed based on the extracted signal DC content in MN1. In the third AOC phase, the loop is set to its slow mode through R_{CTRL} to facilitate signal transition with minimum baseline wander, which is determined by comparing the voltage potential of V_A and V_G nodes. As shown in Fig. 2(c), the BM settling time is only 5.4ns with a large input burst DC current of 2mA. Shown in Fig. 2(d), this AOC is 14× faster than the analog loop without acceleration, and 2× faster than that with the regulated charge pumping (RCP) technique [13], mainly due to the significantly reduced logic control time overhead. In addition, the simplified control also reduces many of charge pump capacitors to save area.

Conventionally, the post-amplifier following the BM-TIA, whether being a standalone chip or as the front-end gain stages of the clock and data recovery (CDR) chip, needs also to be burst-mode, which inevitably raises the design complexity and cost with extra settling time overhead. Though being low-cost thanks to its simplified design, the CM post-amplifier will incur an excessive settling time of tens of microseconds under BM operation in addition to the typical BM post-amplifier. This is because the low-frequency high-pass corner in CM amplifier needs to be sufficiently low (<300kHz) to minimize baseline wander, mandating a large time constant from its input AC coupler or internal CM DC offset cancelation loop, as shown in Fig. 3(a). Our BM-TIA enables a CM post-amplifier to be used under BM operation. The ROC circuit which was originally proposed to suppress the offset transition along the DC coupled signal chain [13]. Here, we explore its application with an AC-coupled CM post-amplifier, as shown in Fig. 3(b). The switch Sc is turned on from the arrival of the BM signal, and the downward signal gain after ROC is essentially reduced along with the offset. The total time constant (τ_{total}) is determined by the smaller one of the two AC couplers in series, in this case $\tau_{on\text{-}chip}$ of around 0.6ns in ROC, enabling a fast BM settling. When the whole AFE is settled, Sc is turned off and $\tau_{on\text{-}chip}$ is restored to a large value of 750ns, forming a τ_{total} of 720ns along with $\tau_{off\text{-}chip}$ for minimum baseline wander. Simulation shows that the maximum ROC ON time is 6ns after FE-TIA is settled, forming a total AFE settling time of 11.4ns.

Figure 4 shows the measurement setup. The BM-TIA is wire-bonded with a commercial 50G PIN-PD in a chip-on-board (COB) optical package. The high-speed signal optical signal comes from a 1.3μm Mach-Zehnder modulator driven by a Keysight M8199A Arbitrary Waveform Generator. A sampling and real-time oscilloscope are used to record the CM and BM output signals. Using the measured noise from the oscilloscope, the gain and bandwidth measured from a lightwave component analyzer (LCA), the obtained IRND is 7pA/√Hz, as shown in Fig. 3(b). Fig. 4(c) shows the measured 50Gb/s differential output eyes at various input optical power. Fig. 5 shows the measured BM transient output signals from the output of the AC-coupled 23dB CM broadband post-amplifier shown in Fig. 4(a). Each burst signal cycle is set to 1us, including 20ns of Preamble, 530ns of payload, and 450ns of guard time. Since the maximum output swing of the post-amplifier is too large, a 20dB attenuator is used to protect the oscilloscope. The settling time measured at the BM-TIA output is around 14ns, which is almost the same as the one obtained from the post-amplifier output. This demonstrates not only fast settling time, but also CM post-amplifier connectivity under BM environment.

Figure 6 compares this work with recent reported high-speed TIAs. State-of-the-art noise performance is achieved in this design with a relative slow technology. The BM-TIA settling time can be 5-10× smaller, and the AFE settling time is 10× smaller. The good performance from bulk CMOS along with its CM post-amplifier connectivity, provides an overall low-cost solution for 50G-PON AFE design. Finally, the die micrograph, power breakdown and its O/E optical PCB are shown in Fig. 7.

2025 IEEE Custom Integrated Circuits Conference (CICC) | 979-8-3315-1745-8/25/$31.00 ©2025 IEEE | DOI: 10.1109/CICC63670.2025.10982699

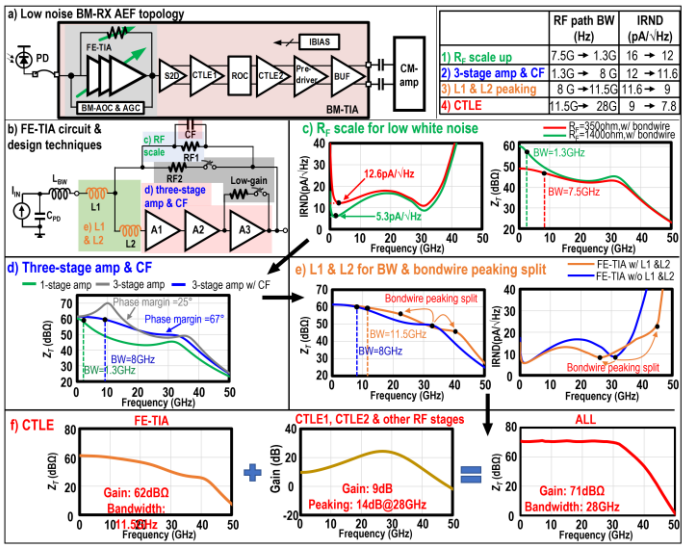

Fig. 1. Low-noise BM-RX AFE topology and RF path design.

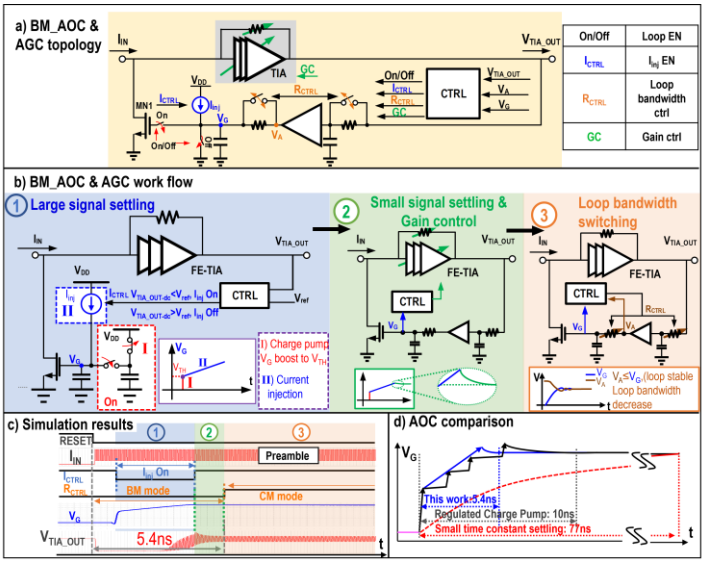

Fig. 2. Fast AOC in BM-TIA.

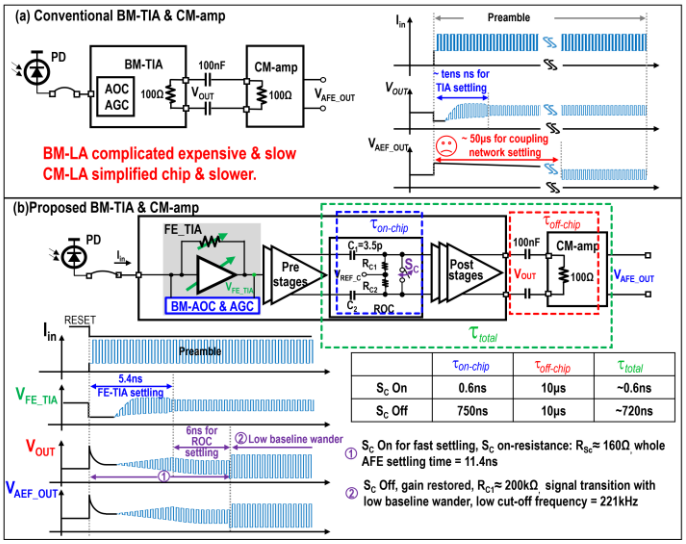

Fig. 3. Design approach for BM-TIA + CM-amp.

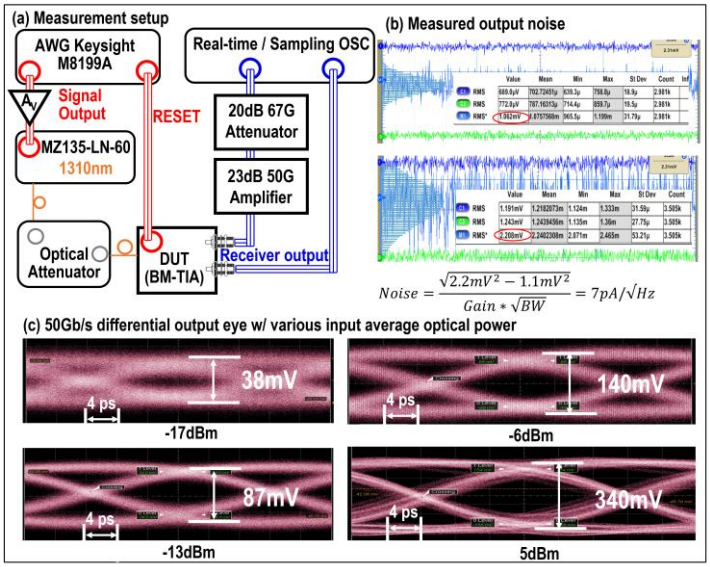

Fig. 4. Measurement setup & output eyes.

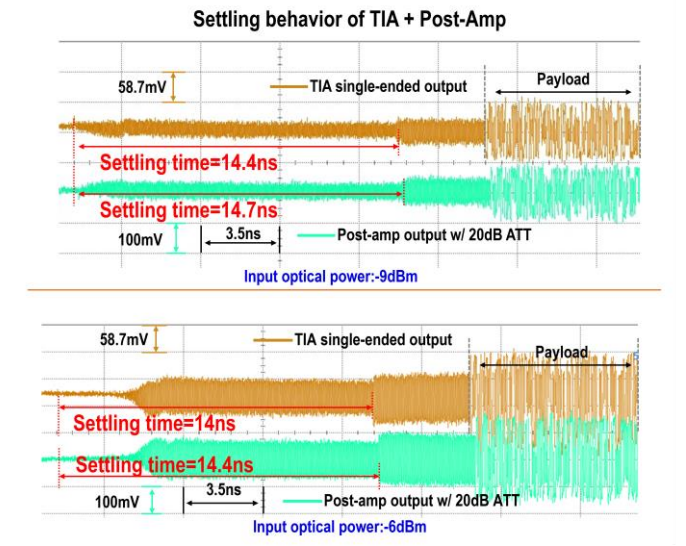

Fig. 5. BM Rx settling behavior.

Published Works	[6] CICC 2024	[7] JSSC 2022	[8] ISSCC 2023	[1] JSSC 2020	[2] JLT 2023	[3] OFC 2023	This work
Baud rate (Gbaud)	56	50	53.125	25	50	25/12.5	**50**
Type	Continuous Mode			Burst Mode			
Technology	22-nm FDSOI CMOS	28-nm CMOS	16-nm FinFET CMOS	0.25 μm SiGe BiCMOS	0.13 μm SiGe BiCMOS	0.13 μm SiGe BiCMOS	**28-nm CMOS**
Post-TIA connectivity	DSP	CDR	DSP	Off-chip BM-amp	On-chip BM-amp	Off-chip BM-amp	**Off-chip CM/BM-amp**
Settling time (ns) 1R^	/	/	/	82.7	/	200	**14.4**
Settling time (ns) 2R*	/	/	/	/	150	/	**14.7**
Bandwidth (GHz)	28^	22.9^^	18.4	17.9	17.1^^^	9.5	**27**
Gain (dBΩ)	74	68.6	75.5	70	80	58.1	**67**
Noise (pA/√Hz)	11	17	7	8.2	N/A	N/A	**7**
Power (mW)	155**	117	108	280	258	N/A	**97.4**
Die area (mm^2)	1.46**	0.9^^	0.64	1.39	2.04	N/A	**0.8**

*AFE settling, **per-channel, ***Electrical, ^ TIA settling, ^^ Estimated ^^^6-dB bandwidth

Fig. 6. Performance comparison of high-speed TIAs.

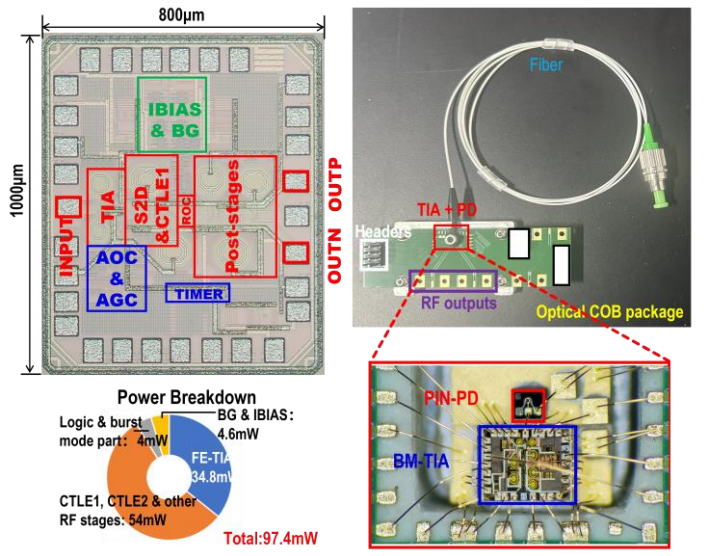

Fig. 7 Die micrograph, power breakdown & optical PCB

Acknowledgements

This work was supported partly by National Key Research and Development Plan under Grant 2022YFB2803301 and the Natural Science Foundation of China under Grant 62074126.

References

[1] G. Coudyzer, P. Ossieur, J. Bauwelinck and X. Yin, "A 25Gbaud PAM-4 Linear Burst-Mode Receiver With Analog Gain- and Offset Control in 0.25μm SiGe:C BiCMOS," in IEEE Journal of Solid-State Circuits, vol. 55, no. 8, pp. 2206-2218, Aug. 2020, doi: 10.1109/JSSC.2020.2987680.

[2] G. Coudyzer et al., "100 Gbit/s PAM-4 Linear Burst-Mode Transimpedance Amplifier for Upstream Flexible Passive Optical Networks," in Journal of Lightwave Technology, vol. 41, no. 12, pp. 3652-3659, 15 June15, 2023, doi: 10.1109/JLT.2023.3262319.

[3] H. Suga, T. Kawanaka, S. Yoshima and S. Shirai, "A simple 25 and 12.5 Gb/s dual-rate burst-mode receiver compliant with ITU-T G.9804.3 N1-class," 2023 Optical Fiber Communications Conference and Exhibition (OFC), San Diego, CA, USA, 2023, pp. 1-3, doi: 10.1364/OFC.2023.Th3G.4.

[4] A. Rylyakov et al., "A 25 Gb/s burst-mode receiver for low latency photonic switch networks," 2015 Optical Fiber Communications Conference and Exhibition (OFC), Los Angeles, CA, USA, 2015, pp. 1-3, doi: 10.1364/OFC.2015.W3D.2.

[5] K. C. Chen and A. Emami, "A 25-Gb/s Avalanche Photodetector-Based Burst-Mode Optical Receiver With 2.24-ns Reconfiguration Time in 28-nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 54, no. 6, pp. 1682-1693, June 2019, doi: 10.1109/JSSC.2019.2902471.

[6] M. Parvizi et al., "A 11 pA/√Hz TIA with +15dB input OMA Range for 112Gb/s PAM4 Optical Links in 22nm FDSOI," 2024 IEEE Custom Integrated Circuits Conference (CICC), Denver, CO, USA, 2024, pp. 1-2, doi: 10.1109/CICC60959.2024.10529083.

[7] H. Li, C. -M. Hsu, J. Sharma, J. Jaussi and G. Balamurugan, "A 100-Gb/s PAM-4 Optical Receiver With 2-Tap FFE and 2-Tap Direct-Feedback DFE in 28-nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 57, no. 1, pp. 44-53, Jan. 2022, doi: 10.1109/JSSC.2021.3110088.

[8] K. Lakshmikumar et al., "A 7 pA√Hz Asymmetric Differential TIA for 100Gb/s PAM-4 links with −14dBm Optical Sensitivity in 16nm CMOS," 2023 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2023, pp. 206-208, doi: 10.1109/ISSCC42615.2023.10067483.

[9] K. R. Lakshmikumar et al., "A Process and Temperature Insensitive CMOS Linear TIA for 100 Gb/s/ λ PAM-4 Optical Links," in IEEE Journal of Solid-State Circuits, vol. 54, no. 11, pp. 3180-3190, Nov. 2019, doi: 10.1109/JSSC.2019.2939652.

[10] D. Li et al., "A Low-Noise Design Technique for High-Speed CMOS Optical Receivers," in IEEE Journal of Solid-State Circuits, vol. 49, no. 6, pp. 1437-1447, June 2014, doi: 10.1109/JSSC.2014.2322868.

[11] D. Li et al., "Low-Noise Broadband CMOS TIA Based on Multi-Stage Stagger-Tuned Amplifier for High-Speed High-Sensitivity Optical Communication," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 66, no. 10, pp. 3676-3689, Oct. 2019, doi: 10.1109/TCSI.2019.2916150.

[12] C. Tan et al., "A 10/2.5-Gb/s Hyper-Supplied CMOS Low-Noise Burst-Mode TIA with Loud Burst Protection and Gearbox Automatic Offset Cancellation for XGS-PON," 2022 IEEE Custom Integrated Circuits Conference (CICC), Newport Beach, CA, USA, 2022, pp. 1-2, doi: 10.1109/CICC53496.2022.9772848.

[13] Y. Xia et al., "An Integrated Burst-Mode 2R Receiver Employing Fast Residual Offset Canceller for XGS-PON in 40-nm CMOS," 2024 IEEE Custom Integrated Circuits Conference (CICC), Denver, CO, USA, 2024, pp. 1-2, doi: 10.1109/CICC60959.2024.10528965.

[14] D. Li, L. Geng, F. Maloberti and F. Svelto, "Overcoming the Transimpedance Limit: A Tutorial on Design of Low-Noise TIA," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 69, no. 6, pp. 2648-2653, June 2022, doi: 10.1109/TCSII.2022.3173155.

[15] X. -Z. Qiu et al., "Fast Synchronization 3R Burst-Mode Receivers for Passive Optical Networks," in Journal of Lightwave Technology, vol. 32, no. 4, pp. 644-659, Feb.15, 2014, doi: 10.1109/JLT.2013.2285594.