CMOS Transimpedance Amplifier for Biosensor Signal Acquisition

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***Abstract*— We present a 1-GΩ CMOS transimpedance amplifier (TIA) suitable for processing sub-nA-level currents in electrochemical biosensor signal-acquisition circuits. Use of a two-stage active transconductor provides resistive feedback in place of a single large-area linear resistor. We engineer the TIA feedback loop to suppress output offset caused by dc input leakage currents of ± 0.9 nA. We also implement a mechanism to tune the low-frequency cutoff of the TIA from 0.7 Hz to 500 Hz which permits operation under variable environmental conditions. We report simulated and experimental results from our custom TIA fabricated in a 3.3-V 0.35-μm CMOS process.**

I. Introduction

Resistor- and capacitor-feedback transimpedance amplifiers (TIAs) for measuring nA-level currents and below have found numerous applications in CMOS-integrated electrochemical biosensors, including patch-clamp electrophysiology chips [1][2], integrated nanopore and ion channel sensors [3][4][5], and on-chip electrochemical DNA sensor arrays [6][7]. In a typical electrochemical biosensor, the TIA holds the working electrode where the biochemical reaction of interest occurs at virtual ground and converts the input signal current to an amplified voltage to enable further gain and signal processing. The high TIA gain reduces input-referred current noise so that an adequate biosensor detection limit can be achieved.

A desirable function of the TIA is to prevent the passage of large offset voltage caused by input leakage current from the biochemical process under investigation and external low-frequency interference. This offset could saturate subsequent stages of the acquisition circuit, reducing dynamic range. While ac coupling subsequent stages can prevent saturation, integration of large dc-blocking capacitors may be impractical due to chip area constraints. To combat this issue, a CMOS integrator-differentiator-based TIA with a continuous-time capacitor reset network for impedance spectroscopy has previously been reported which prevents saturation of the first-stage integrator [8]. In addition, a TIA constructed from discrete components for semiconductor radiation detection has been reported which uses a proportional-integral control amplifier in the feedback path to zero the dc level of the TIA output [9].

We present a 1-GΩ CMOS resistive-feedback TIA with adjustable low-frequency cutoff. Our design is intended for use in electrochemical impedance spectroscopy (EIS) biosensor applications to record nA-level ac currents in the 1-Hz to 1-kHz range. Unlike [9], our TIA is amenable to CMOS integration because we integrate a two-stage op-amp-based transconductor [10] to achieve 1-GΩ transimpedance. Use of a single linear resistor to achieve such high gain would consume excessive chip area. In addition, while [8] and [9] are effective in reducing TIA output offset, no mechanism is provided to adjust the low-frequency cutoff in a continuous fashion to adapt to changes in measurement conditions. Our work, however, supports frequency tuning by adjusting a MOS active resistor through gate-voltage control within the TIA feedback loop.

In Section II, we present system-level considerations and the TIA architecture. Circuit design and implementation details are discussed in Section III. In Section IV, we present experimental results from our proposed TIA implemented in a five-metal, two-poly, 0.35-μm CMOS process. Section V concludes the paper.

II. Circuit Architecture

We achieve high transimpedance (gain) using an active transconductor in the feedback loop instead of a single large linear resistor. A conventional TIA with feedback resistor R_f is shown in Fig. 1(a). The overall transimpedance $v_{OUT}/i_{IN} = -R_f$, where v_{OUT} is the total output voltage and i_{IN} is the total input current. Fig. 1(b) shows a simplified diagram of our TIA architecture, in which active transconductor G_m provides a feedback resistance $R_f = 1/G_m$.

A. Feedback Transconductor

The two-stage transconductor in Fig. 1(b) is formed using amplifiers A_3 and A_4 and resistors R_b and MR_b, where M is a multiplicative factor. Current i_{OUT} is converted to v_{OUT} using resistor R_a. Since the current through R_b is M times larger than the current through MR_b, use of two transconductance stages gives $i_{OUT} = i_{IN}M^2$. This current gain provides a large $1/G_m$ such that the overall TIA gain is $-M^2R_a$. In contrast to [10], we use linear resistors in the feedback transconductor instead of MOS-bipolar pseudo-resistors to improve linearity at the expense of noise performance.

B. Low-Frequency Input Signal Suppression

We also suppress the effects of low-frequency input currents by zeroing the output dc level of the TIA using the non-inverting integrator composed of amplifier A_2, resistor R_2, and

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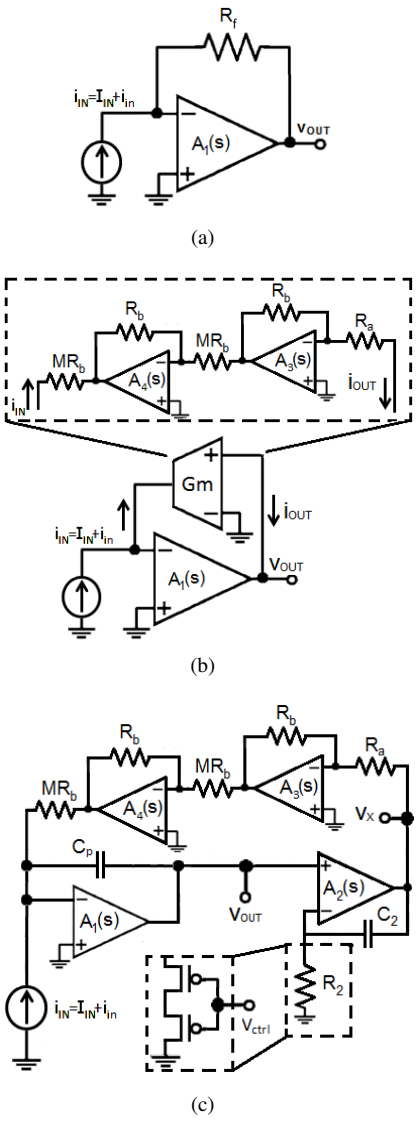

Fig. 1. Transimpedance amplifier with (a) linear feedback resistor, (b) two-stage feedback transconductor, and (c) integrator to suppress input currents below the low-frequency cutoff.

capacitor C_2 shown in Fig. 1(c). The low-frequency behaviour of the TIA is established by the zero and pole generated by integrator time constant R_2C_2. For input-signal frequencies near the low-frequency cutoff $f_L = 1/(2\pi R_2 C_2)$, the TIA small-signal gain is given by

$$\frac{v_{out}(s)}{i_{in}(s)} \approx -\frac{1}{G_m A_{2_0}} \frac{1 + sR_2C_2A_{2_0}}{1 + sR_2C_2}, \tag{1}$$

where A_{2_0} is the open-loop dc gain of A_2. As shown in the above equation, the pole and zero are separated by a factor A_{2_0} and the TIA gain is attenuated by the same factor. At input-signal frequencies below f_L, the impedance of C_2 becomes very large, which causes the small-signal voltage gain v_x/v_{out} to be nearly A_{2_0}, where v_x is taken from the A_2 output as shown in Fig. 1(c). Therefore, the small-signal transimpedance v_x/i_{in} is still $1/G_m$ and is prone to saturation due to dc input current.

Conversely, input signals at frequencies above f_L propagate directly to v_{OUT} as A_2 operates in a unity-gain configuration at these frequencies. However, A_2 prevents the passage of offset voltage to v_{OUT} due to dc input current. Fig. 1(c) also illustrates the parasitic capacitance C_p in parallel with the feedback transconductor which affects the high-frequency response of the TIA. We estimate C_p to be on the order of 100 fF in our design. At frequencies greater than f_L, the TIA small-signal gain is given by

$$\frac{v_{out}(s)}{i_{in}(s)} \approx -\frac{1}{G_m} \frac{1}{1 + sC_p/G_m}, \tag{2}$$

which shows the high-frequency cutoff of the TIA. Fig. 2 displays the expected magnitude of the TIA frequency response.

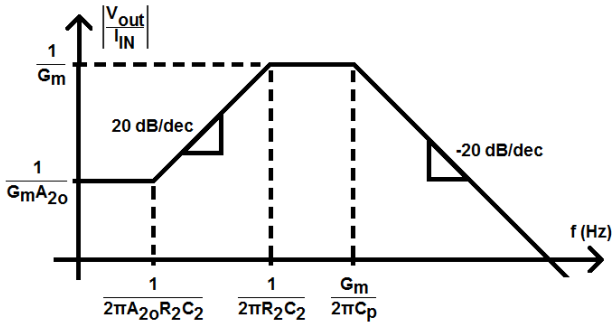

Fig. 2. Expected magnitude of TIA frequency response.

III. Circuit Design

The complete TIA with active resistor for tuning the low-frequency cutoff is shown in Fig. 1(c). On-chip voltage buffers (not shown), designed to drive a 50-pF load capacitance with a 60° phase margin, transmit outputs v_{OUT} and v_X off chip.

A. Bandwidth Tuning

We tune the TIA bandwidth to suppress low-frequency input signals by implementing R_2 using an active resistor comprised of two identical series PMOS transistors operated in the subthreshold regime as shown in Fig. 1(c). The effective resistance of these devices is controlled by adjusting the gate voltage V_{ctrl} using an external dc source. Fig. 5 shows the simulated variation in f_L as the control voltage of the active resistor changes. With $C_2 = 10$ pF, f_L can be varied from less than 1 Hz to more than 10 kHz.

B. Transconductor Design

We have designed a two-stage feedback transconductor with $M = 150$ and $R_a = 50$ kΩ to obtain a nominal transimpedance of $M^2R_a = 1.125$ GΩ. We use p-implant resistors (with resistivity 150 Ω/sq) to implement $R_b = 10$ kΩ and $MR_b = 1.5$ MΩ due to the more aggressive n-well spacing rules. The total chip area occupied by resistors in the transconductor is 0.23 mm^2. This is much more area efficient than implementing a single 1-GΩ resistor using unit-size resistors.

C. Amplifier Design

Table I summarizes the simulated performance of each amplifier used in the TIA under typical process corners. The loop gain of the system is given by $G_{loop} \approx \frac{A_{1_0} R_b}{M R_a}$. Since the multiplication factor M and R_a have already been set by the gain, and increasing R_b requires more chip area, A_1 has been tuned in order to boost the loop gain. We implement A_1 using two identical folded-cascode amplifiers (denoted A_{1a} and A_{1b}) in cascade each with a dc gain of 70 dB to provide sufficient loop gain to regulate the virtual ground at the TIA input.

TABLE I

SIMULATED PERFORMANCE OF INDIVIDUAL AMPLIFIERS IN TIA.

Parameter	A_{1a}/A_{1b}	A_2	A_3	A_4
Architecture	folded cascode	3-stage	2-stage	folded cascode
Open-loop dc gain (dB)	70	100	82	83
3-dB bandwidth (Hz)	5600	56	1130	1020
Phase margin (deg)	59	68	46	40
Load capacitance (pF)	0.3	1.0	-	-
Load resistance (kΩ)	-	50	1500	-
Power (mW)	1.38	1.11	1.85	1.18
Output swing (V)	1.0	3.0	1.3	1.3

Amplifier A_2 consists of three stages: a PMOS input cascode stage, source follower, and PMOS common-source (CS) amplifier. The source follower is used to provide a positive voltage level shift at the gate of the CS input to ensure that this stage operates in saturation. It is sized to reduce the CS overdrive voltage thereby enhancing the output swing. The CS stage contributes additional gain and is also sized to drive resistive load R_a. The dc gain of A_2 is 100 dB to ensure the attenuation of dc signals between v_X and v_{OUT}. The amplifier gain is enhanced due to the increased output resistance provided by 2-μm-channel-length devices in the cascode stage. The 3-dB bandwidth of A_2 is 56 Hz to maintain stability under unity-feedback operation.

Amplifiers A_3 and A_4 have an identical folded-cascode input stage but A_3 also includes an output stage to drive R_b. Amplifier A_4, however, does not require an output stage because it must deliver only nA-level dc currents.

IV. EXPERIMENTAL RESULTS

We have implemented our TIA in a five-metal, two-poly, 3.3-V 0.35-μm CMOS process. The fabricated chip is shown in Fig. 3 where the TIA occupies an area of approximately 0.68 mm^2.

Fig. 4 shows the frequency response of the TIA for different values of the f_L tuning voltage. As V_{ctrl} increases, the resistance of the PMOS active resistor also increases which reduces f_L. The measured transimpedance of the system is approximately 184 dB (1.58 GΩ). The 40% relative error between the targeted and measured gain is due to mismatch between resistors R_b and MR_b, as well as the deviation in R_a from its designed value due to tolerances in the fabrication process.

Input signal currents at frequencies below f_L are attenuated at a rate of 20 dB/decade. This decay should continue to a minimum of approximately 84 dB (the difference between the passband gain and open-loop gain of A_2) which is not apparent from the measured data because the output signal drops below the system noise floor at very low frequencies. As V_{ctrl} increases from 0.85 V to 1.2 V, f_L is reduced from 500 Hz to 0.7 Hz. This variation is in agreement with the simulated results in Fig. 5.

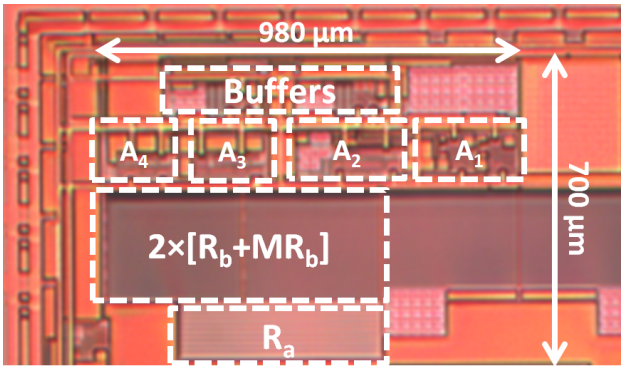

Fig. 3. Chip photo showing key TIA components.

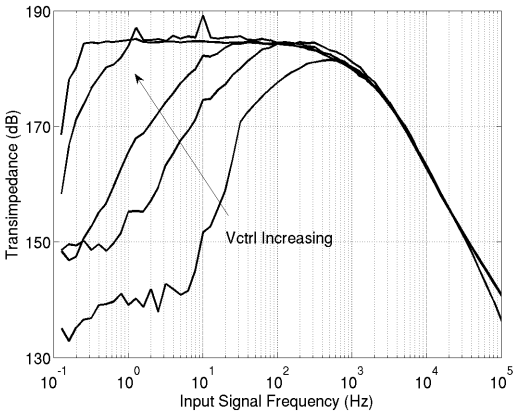

Fig. 4. Measured transimpedance over frequency with variable low-frequency cutoff.

The measured high-frequency cutoff of the TIA is approximately 650 Hz. With the measured transimpedance of 1.58 GΩ, C_p is estimated to be 150 fF. For impedance spectroscopy applications requiring higher input signal frequencies, the TIA bandwidth can be increased by effectively reducing $1/G_m$.

Fig. 6 shows the ac output voltage as a function of a 200-Hz input current signal to illustrate the TIA linearity. At an input current of approximately 0.8 $\mathrm{nA_{pp}}$, the output v_{OUT} starts to saturate. This results from the nonlinear behaviour of the active resistor for large output voltage swings. The slope of the best-fit line to the measured data indicates a transimpedance of approximately 1.79 GΩ before saturation occurs, which is nearly that measured from the frequency response in Fig. 4. Fig. 6 also shows that the relative linearity error does not exceed 1.1% over an input current range from 0.2 $\mathrm{nA_{pp}}$ to 0.8 $\mathrm{nA_{pp}}$.

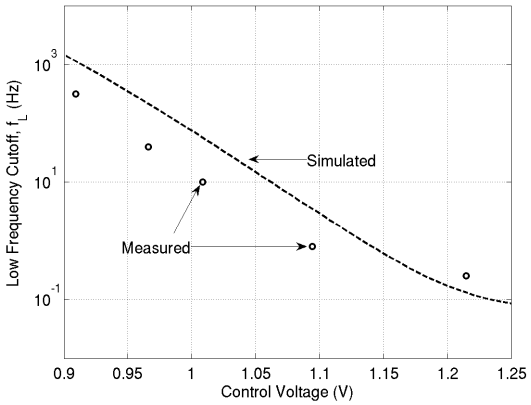

Fig. 5. Simulated and measured tuning range of the TIA low-frequency cutoff.

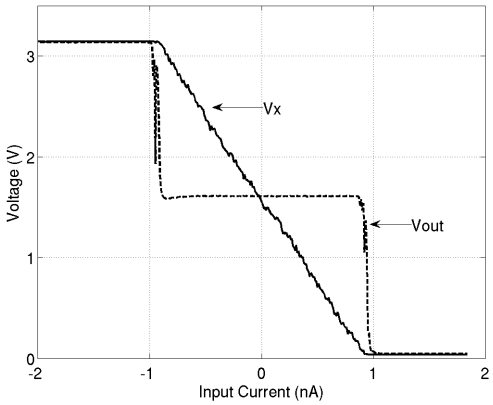

Fig. 7. Measured dc outputs from TIA v_{OUT} and v_X as a function of dc input current.

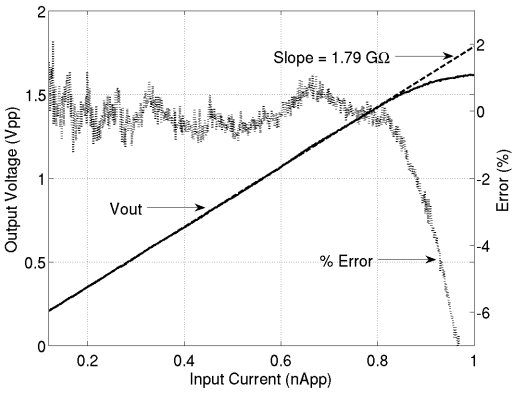

Fig. 6. Measured relative linearity error of the TIA with an ac input current.

Fig. 7 shows the measured v_{OUT} and v_X for positive and negative dc input currents. Output v_X follows the current with a constant slope equal to the transimpedance gain because the low-frequency part of the input signal is not attenuated at this node. The TIA can process a dc current of ± 0.9 nA before v_X saturates at the supply rails. However, v_{OUT} is regulated at the 1.65-V common-mode level over the input current range due to the low-frequency suppression.

The measured power spectral density of the TIA input-referred thermal noise current is approximately $0.4\ \mathrm{pA}/\sqrt{\mathrm{Hz}}$, which is about four times greater than the theoretical thermal noise floor established by resistor MR_b connected to the TIA input node in Fig. 1(c). The total measured and simulated input-referred current noise of the TIA over a bandwidth from 1 Hz to 10 kHz is 52 $\mathrm{pA_{rms}}$ and 35 $\mathrm{pA_{rms}}$, respectively, which is dominated by amplifier flicker noise. We believe the additional measured noise compared to simulation is due to excess noise produced by our measurement setup.

V. Summary

We have presented a CMOS TIA having a measured gain of 1.58 GΩ suitable for low-current electrochemical biosensors. Use of a feedback transconductor instead of a single linear resistor to achieve high gain results in chip area savings. We have also suppressed the effect of undesirable input leakage currents on the output. By using an active resistor in the feedback path, we have achieved a tunable low-frequency cutoff ranging from 0.7 Hz to 500 Hz.

Acknowledgment

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