A Dual-Mode Adjustable High-Gain Ultra-Low Noise Transimpedance Amplifier for Fine Dust Detection

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***Abstract*— This paper presents a dual-mode adjustable-high-gain transimpedance amplifier (TIA). The TIA is designed with a high sensitivity to current bio-signals for a fine-dust detection system Integrated Circuit (IC) based on the operation of a photodiode module with high gain amplifications. Gain adjustment is implemented by coarse gain steps using selective-loads with four different gain values and fine gain steps by 42 dBΩ during 16 fine steps. To improve the settling time, a capacitive compensation is applied for the last stage. An off-state circuitry is proposed to avoid any off-current leakage. This TIA is designed in a 0.18 µm standard CMOS technology, output reached high gains from 149 dBΩ up to 216 dBΩ with 67 dBΩ gain variation range, input referred noise less than 600 fA/ √ Hz in low frequencies and less then 27 fA/ √ Hz at 20 KHz, a minimum detectable current signal of 4 pA, and has a power consumption of 2.71 mW.**

Keywords—dual-mode gain, ultra-low-noise, transimpedance amplifier, TIA, high gain, high sensitive

I. INTRODUCTION (*HEADING 1*)

One of critical issues in human's modern life is the air pollution due to the industries, transfer vehicles, and etc. The particles less than 2.5 µm in width are known as fine particulate matter or PM_2.5. Detection of fine dust particles by a photodiode module (PD) requires a low noise amplification for nA currents of PD's front-end. This amplification is provided by a low-noise transimpedance amplifier (TIA). A very low-noise TIA for the fine-dust detection requires having high-gains within a small bandwidth due to the low frequency bio-signals. In light current operation of PD, the TIA experiences large amounts of currents in µA range. The saturation of TIA's output can be avoided by gain-adjustment of the TIA to increase the input dynamic range and improving the sensitivity consequently.

Tuning the output voltage of the TIA works as the fine adjustment of output voltage, which is interesting in the term of the system level implementation of the bio-sensing system. In [1], gain variable TIA is implement based on shunt-shunt feedback resistor to change the gain of the TIA through the variable on resistances. However, different on resistances also directly affect the input impedance of the TIA and it may change the responsivity of PD when its load condition is changing. In [2], variable transimpedance gain is implemented for TIA by adjustable load resistors. The selective loads are located between first and second stages, which does not have loading effect at output node. Fig. 1 shows the block diagram of the sensing part of a fine-dust bio-system, which is formed by a photo diode module and the TIA. The photo diode module produces very small current signals, which it is proportional to the density of passing dust through the module.

II. PROPOSED TIA

The proposed TIA with dual-mode transimpedance gain is shown in Fig. 2. Digitally controlled Selective-Loads are formed the coarse variable-gain of the TIA through the K1 to K4 switches. The reason of such implementation for variable gain mechanicism is the separation of the selective-loads from input and output branches that prevents any change in input and output impedances. Second gain adjustment works by controlling bias voltage of the gate of the M8 which is called fine gain steps control. The novelty of this work is to implement and control the coarse and the fine gain steps by two separated gain adjustment mechanisms using individual control bits. Fig. 3 illustrates the block diagram of the control unit of fine gain steps, which produces 16 individual tuning voltages to bias M8.

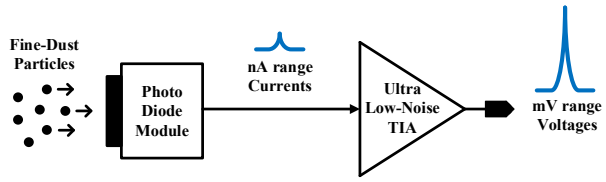

Fig. 1. Fine-Dust particles detection and signal amplification processes through the photo-diode module and ultra-low-noise TIA respectively.

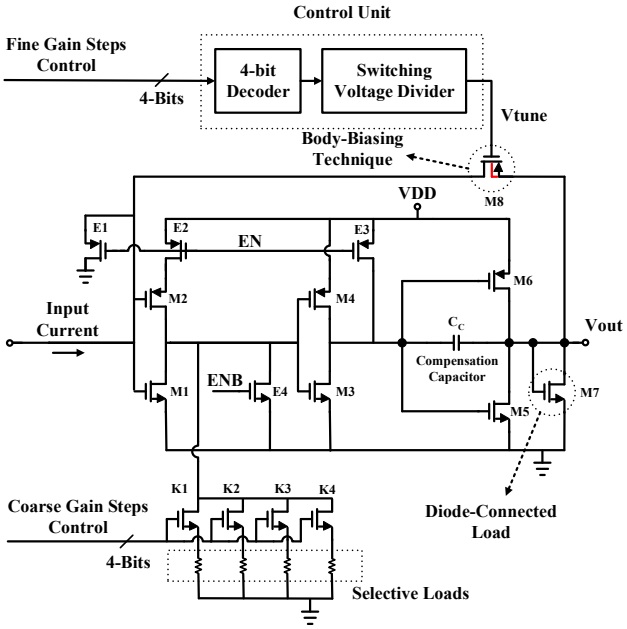

Fig. 2 The proposed TIA with the fine and coarse gain steps mechanisms, body biased feedback transistor, compensation, off-current circuitry, and the diode-connected load.

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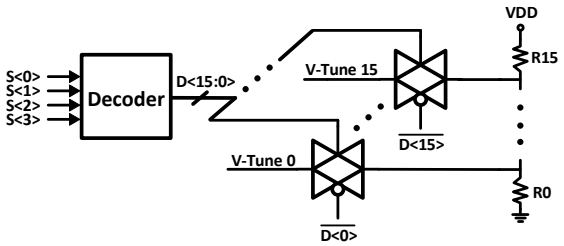

Fig. 3 The proposed TIA sub-blocks in Top Layout.

The M8 transistor is designed using body-biasing technique which results in a considerable reduction of the total input referred noise of the TIA. To obtain high levels of gain, core of the TIA is implemented by three push-pull CMOS inverting amplifier stages [3], [4]. A diode-connected transistor is used as the load of the third stage. A compensation capacitor (C_C) is used to improve the settling time of the TIA when the phase margin is adjusted to 60 degree.

To reach high sensitivity for very small input currents of the TIA considering main contributing resources of input-referred noise could be effective. The equivalent input-referred noise of the TIA can be obtained and it is independent from selective-loads as bellow:

$$e_{eq} = \sqrt{\left(\frac{g_m e_{n1}}{g_{m1}+g_{m2}}\right)^2 + \left(\frac{g_{m2} e_{n2}}{g_{m1}+g_{m2}}\right)^2} \qquad (1)$$

Where ${e_{n1}}^2$ and ${e_{n2}}^2$ are input-voltage noise spectral density at the gates of M1 and M2 respectively. It means that total noise contribution can only be reduced by reducing the noise contribution of each device. A nomograph technique introduced by [4] is followed to specify the optimal size of transistors for low noise operation.

Due to complexity of the off-state of cascaded inverting amplifiers, an off-state circuitry is proposed to avoid any off-current leakage. The proposed off-state circuitry is implemented through the E1 to E4 transistors which states the operation ON when EN is HIGH (ENB is LOW) and vice versa as shown in Fig 2. The selective loads are placed between the first and the second stages of the TIA to implement the coarse gain steps which their effect on the gain of the first stage (A1) is reflected by g_L as follow:

$$A_1 = \frac{-(g_{m1}+g_{m2})}{g_{ds1}+g_{ds2}+g_L} \qquad (2)$$

Where $g_{m1,2}$ and $g_{ds1,2}$ are transconductance and channel conductance of M_1 and M_2 transistors respectively, g_L is the conductance controlled by selective-loads. Overall bandwidth of the TIA is affected by the pole of the first stage (P_1) as an approximated equation (3) which $C_{gd1,2}$ and $C_{bd1,2}$ are gate-drain and bulk-drain parasitic capacitances respectively due to the M_1 and M_2 transistors.

$$P_1 = \frac{-(g_{ds1}+g_{ds2}+g_L)}{C_{gd1}+C_{gd2}+C_{bd1}+C_{bd2}} \qquad (3)$$

III. Simulation Results

The proposed TIA is designed in a standard 0.18 µm CMOS technology which occupies 87 µm × 125 µm of the chip. Top layout of the TIA is depicted in Fig. 4. Fine-gain steps are provided through 16 different levels of tune-voltages to bias M8 transistor to control its on resistance consequently. Fig. 5 shows the gain variation range of the fine gain steps which results in a 42 dBΩ range during 16 individual steps of fine gain control. Monte-Carlo analysis for the total input referred noise result in a maximum input-referred noise variation of 150 fA/ √ Hz in very low frequencies as shown in Fig. 6. Coarse gain steps which are implemented through four individual loads result in a 67 dB gain variation range during 4 coarse gain steps from 149 dBΩ to 216 dBΩ which is depicted in Fig. 7. In term of the input referred noise analysis, post-layout simulation in all process corners considering all gain states shows that it is less than 600 fA/ √ Hz in low frequencies and less than 27 fA/ √ Hz at 20 KHz.

Post-layout simulation shows the sensitivity of the TIA is very high which can amplify the currents as small as 4 pA signals with a high gain which is illustrated in Fig. 8. The response of 1.32 mV to 4 pA input current results in 170 dBΩ gain for this case. Due to the high sensitivity of the TIA all of the environment effects of the chip including pad of the chip and its bound wires are considered by using proper models in the test-bench of post-simulation to guarantee satisfying results for the real application. Table 1 shows a comparison of the proposed TIA with similar works.

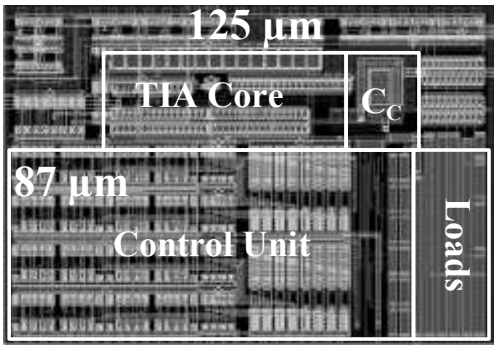

Fig. 4 Top layout of the proposed TIA.

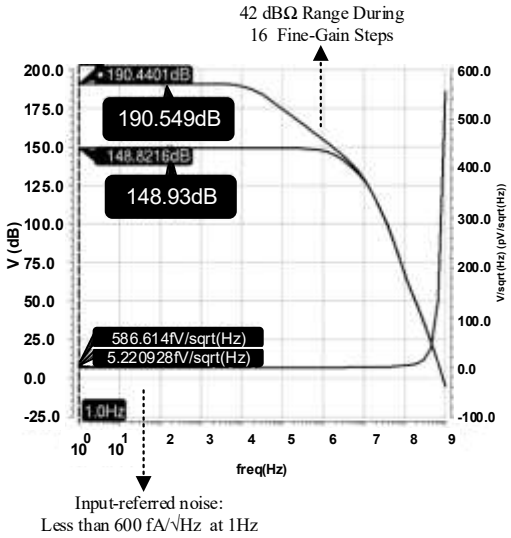

Fig. 5. Gain variation range of the fine gain steps during 16 individual fine steps.

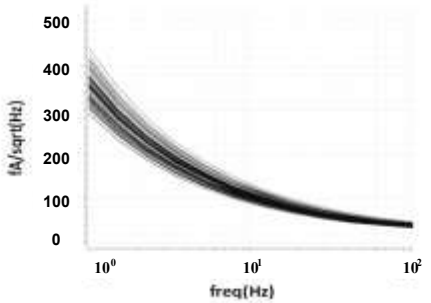

Fig. 6. Monte-Carlo analysis for the total input referred noise.

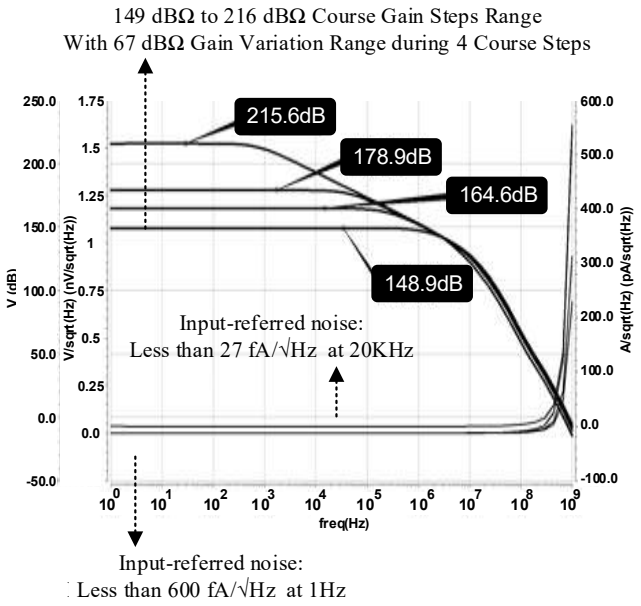

Fig. 7. Coarse gain steps during 4 individual coarse steps and input-referred noise.

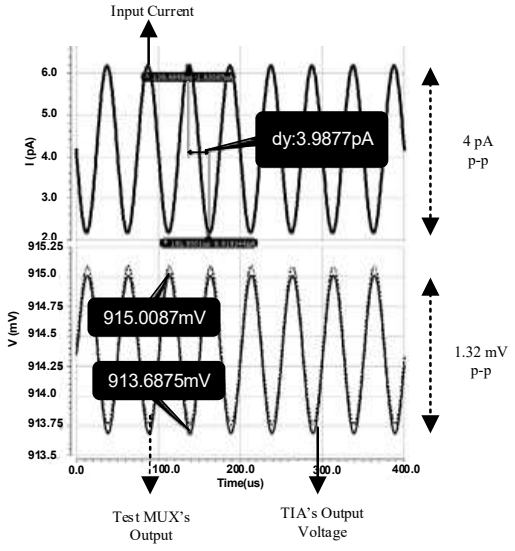

Fig. 8. Post-layout input/output simulation results for 4 pA p-p input current considering environment effects of the chip.

TABLE I. COMPARISON TABLE

Design of TIA	[2]	[3]	[4]	[5]	This Work
Process Technology	0.18 µm CMOS	0.35 µm CMOS	0.35 µm Si CMOS	0.18 µm CMOS	0.18 µm CMOS
Supply (V)	3.3	1.8	NA	1.8	3.3
Topology	Common-Mode Amplifier	Shunt feedback amplifier +	3-stage push-pull inverters	Dual-mode CMOS feed-forward	Adjustable-Gain 3-stage Push-pull inverters
C_{PD} (pF)	2	0.5	10	0.5	1
Gain (dBΩ)	52-106	50-65	107.3	76	149-216
Coarse Gain-Step Range (dBΩ)	54	15	-	-	67
Fine Gain-Step Range (dBΩ)	-	-	-	-	42
Power Consumption (mW)	8	6.2	60	20.7	2.71
Area (μm^2)	283.8k	NA	15.9k	117.5k	10.9k

IV. CONCLUSION

The proposed dual-mode adjustable-high-gain TIA is designed in a 0.18 µm standard CMOS technology. The TIA has a coarse gain steps from 149 dBΩ to 216 dBΩ with 67 dBΩ gain variation range during 4 steps. The input referred noise is less than 600 fA/ √ Hz in low frequencies and less than 27 fA/ √ Hz at 20 KHz in all process corners of post-layout simulation. The fine gain steps have 42 dBΩ gain variation range during 16 individual fine steps. The minimum detectable current signal is 4 pA with 170 dBΩ transient gain and the power consumption of 2.71 mW.

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