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Interleaving Active Feedback in Inverter-Based Optical Receivers for Bandwidth Extension and Linearity Improvement

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***Abstract*— Main amplifiers are crucial components in the design of optical receivers, amplifying the output voltage of the transimpedance amplifier (TIA). While Cherry-Hooper (CH) amplifiers are widely utilized in optical receivers due to their high bandwidth, they often fall short in linearity, making them less suitable for PAM-4 and higher-order modulation schemes. This study presents a highly linear PAM-4 optical receiver design. The proposed main amplifier employs g_m/g_m inverter-based amplifiers known for their superior linearity. We have applied the interleaving active feedback (IAFB) technique to enhance bandwidth while mitigating gain peaking. Notably, our proposed design operates with a 1 V supply, offers a bandwidth of 20 GHz at a gain of 64 V/V, and achieves a total harmonic distortion (THD) of less than 1% for a 600 mV_{pp} differential output swing.**

Keywords—Cherry-Hooper amplifier, g_m/g_m amplifier, inverter-based, IAFB, main amplifier, linearity, PAM-4, optical receiver

I. Introduction

Due to the massive data volumes generated in modern data centers, electrical interconnects often become bottlenecks; adopting optical interconnects over electrical ones has become crucial. On the other hand, optical interconnects use light signals to transmit data, enabling faster, more reliable, and lower power communication.

When it comes to increasing the data rate using intensity modulation and direct detection (IMDD) transceivers, the practicality of two-level pulse amplitude modulation (PAM-2) is limited, due to the requirement of extremely large bandwidths. As a result, higher-order modulation formats such as PAM-4 have become popular. PAM-4 uses four discrete signal amplitude levels to encode two information bits per symbol, allowing for a higher data transmission rate than PAM-2, resulting in reduced bandwidth requirements for the same level of performance [1]. However, PAM-4 involves inevitable trade-offs. Firstly, four amplitude levels mean there is less separation between the levels, making it easier for noise and distortion to affect the accurate detection of the symbol. The second consideration is that an analog front-end with high linearity must be designed to produce four equally spaced levels [1].

The nonlinearity of the optical receiver is primarily caused by the main amplifier. The Cherry-Hooper (CH) amplifier is one of the common topologies [2, 3] because of its wide bandwidth. However, in [4], it is shown that the linearity of CH amplifiers is not high enough, especially for PAM-4 optical links. To improve linearity, [4] uses g_m/g_m amplifiers that consist of a transconductor followed by a diode-connected inverter load to cancel the nonlinearities of the transconductor [5]. Although the g_m/g_m topology is highly linear, its bandwidth is much smaller than a CH amplifier. In less advanced technologies, the g_m/g_m design will require bandwidth extension techniques [6-10].

This paper proposes a highly linear PAM-4 optical receiver based on the g_m/g_m topology in 65 nm CMOS technology. The interleaving active feedback (IAFB) technique [6] improves the bandwidth without using passive inductors. A combination of g_m/g_m main amplifiers and the IAFB technique has yielded an optical receiver with a data rate of 50 Gb/s (25 GBaud/s) with a total harmonic distortion (THD) of less than 1% at 600 mV_{pp} differential output swing. Section II discusses the design of the proposed optical receiver. In Section III, the simulation results are presented. Finally, Section IV concludes the paper.

II. Design Description

The initial stage of a standard CMOS optical receiver comprises a photodiode and a transimpedance amplifier (TIA). A TIA converts an input current into an output voltage. Then, we need to use the main amplifiers to amplify the TIA's output voltage to have sufficient amplitude. This section discusses the properties of the analog inverter to be used as main amplifiers in an optical receiver chain.

When an analog inverter (Fig. 1(a)) is biased at the midpoint between the maximum and minimum power supply voltages, both the n-channel and p-channel transistors operate in the saturation region. In this condition, the inverter has the maximum possible gain and serves as a linear transconductor [11]. The overall transconductance of the block is the result of adding the small-signal transconductance of both NMOS and PMOS transistors. This simple two-transistor circuit has only two nodes, i.e., input and output nodes. Therefore, it removes the concern of additional parasitic poles that might degrade the bandwidth [4]. The efficiency of the analog inverter transconductor in terms of noise, power consumption, and bandwidth, all while maintaining a satisfactory level of linearity performance, has made it a foundational cell that can be applied to accomplish various functions [5, 12, 13]. The output current of the transconductor of Fig. 1(a) can be written as:

$$i_o = i_n - i_p \approx \left(k_n V_{ov,n} + k_p V_{ov,p}\right) v_i + \left(\frac{k_n}{2} - \frac{k_p}{2}\right) v_i^2 \qquad (1)$$

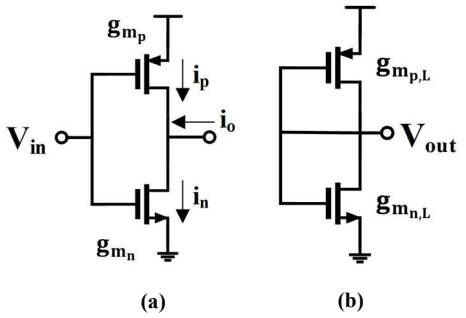

Fig. 1. Schematic diagram of (a) a transconductor, and (b) shorted inverter.

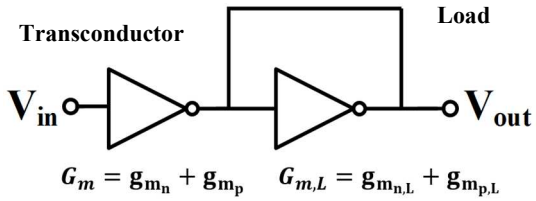

Fig. 2. Block diagram of the g_m/g_m amplifier.

where $k = \mu C_{ox}(\frac{W}{L})$ and $V_{ov} = V_{GS} - V_t$. The current-voltage equation shows that if $k_n = k_p$, the second-order nonlinearity cancels out. In the event of a mismatch, the second-order nonlinearity is only proportionate to $k_n - k_p$. Mobility degradation caused by the transverse electric field and channel length modulation results in the creation of odd-order nonlinearities. These nonlinearities can pose challenges, especially when operating in low-supply voltages [4]. Fig. 1(b) represents a shorted inverter. [4] demonstrates that an inverter-based transconductor loaded with a diode-connected inverter called a g_m/g_m amplifier (Fig. 2), offers much better linearity compared to the CH amplifiers. The reason for calling it a g_m/g_m amplifier is that the total gain of the block in Fig. 2 is equal to $G_m/G_{m,L}$ where G_m and $G_{m,L}$ denote the total transconductances of the transconductor and load stages, respectively. A detailed discussion of the higher linearity of the g_m/g_m amplifier can be found in [11]. When NMOS and PMOS transistors have nearly equal threshold voltages, negligible channel length modulation, and operate in saturation, the output voltage of the unity gain g_m/g_m amplifier in Fig. 2 can be expressed as [14]:

$$V_{out} = V_{DD} - V_{in} \tag{2}$$

which shows a linear input-output relationship as a buffer, assuming square-law operation of the MOSFETs.

Based on the discussion above, the g_m/g_m amplifier can be an excellent candidate to be used as a linear main amplifier. However, compared to the CH amplifier, it has a small bandwidth because of the repeated real poles of a cascaded g_m/g_m amplifier, which compresses the bandwidth more than the second-order CH amplifier. Therefore, bandwidth extension techniques must be applied to the main amplifier to compensate for that. In general, implementing negative feedback can improve both the bandwidth and linearity of a circuit. Poles can be shifted to higher values, and pole Q can be improved by introducing negative feedback, thereby extending the bandwidth [6]. As nonlinearity can be perceived as fluctuations in the small-signal gain with the input level, negative feedback is also anticipated to suppress such variations, resulting in improved linearity for the closed-loop system [3]. [6] introduces the IAFB technique to enhance the bandwidth of the cascaded third-order amplifier cells through the pole-splitting phenomenon. While negative active feedback can improve bandwidth, it can increase gain peaking [6]. Nevertheless, the IAFB technique can increase bandwidth with reasonable gain flatness through a combination of low and high Q pole pairs.

Fig. 3 shows the proposed linear amplifier based on the g_m/g_m amplifier and the IAFB technique. This configuration comprises six stages of inverter-based transconductors, known for their high linearity, loaded by diode-connected inverters, and employs IAFB to boost bandwidth. Notably, this design exhibits considerably superior linearity compared to a six-stage cascade of CH amplifiers with equivalent input voltage and gain. Furthermore, the IAFB approach has led to a broader bandwidth when compared to its CH amplifier-based counterpart. The subsequent section delves into the design methodology and simulation results of the proposed PAM-4 main amplifier and offers a comparison with the widely employed CH amplifier.

III. Design Methodology and Simulation Results

A. PMOS to NMOS Ratio

The proposed linear main amplifier is designed in 65 nm CMOS technology. It operates with a 1 V supply voltage. Let us first consider Fig. 3 without any feedback. In the open-loop design, each g_m/g_m cell is designed to have a gain of 2. In advanced technology like 16 nm FinFet, the n-channel and p-channel transistors have identical mobility and threshold voltage. Moreover, the g_m of the transistors is about 10 times larger than g_{ds}, which makes it possible to ignore channel length modulation [14]. Hence, if the size of the load inverter in Fig. 2 is reduced to half that of the transconductor, achieving a gain of 2 is straightforward. However, in 65 nm CMOS technology, the mobility of the NMOS and PMOS transistors is not the same, and g_{ds} must be considered in the calculations.

Based on our simulations, the g_m/g_m amplifier has the highest linearity when the PMOS transistor's width is 2.5 times larger than NMOS's. Therefore, considering this ratio and channel length modulation, in the open-loop design, the width of NMOS in the transconductor and load inverters is 10 µm and 2.7 µm, respectively. The PMOS transistors are 2.5 times larger than their corresponding NMOS transistors. Using these dimensions, each g_m/g_m amplifier in Fig. 3 has a gain of 2, giving a total gain of 64 for the six cascaded g_m/g_m amplifiers.

B. Gain Selection

The next step is to add the negative active feedback and the IAFB to the circuit, which both consist of single inverters. To have a reasonable comparison, using (3) [6], the total gain of the proposed circuit is kept at 64 by increasing the gain of each g_m/g_m cell:

$$H(s) = \frac{G^6(s)}{1 + 3G^2(s)G_f(s) + G^4(s)G_f^2(s)}. \tag{3}$$

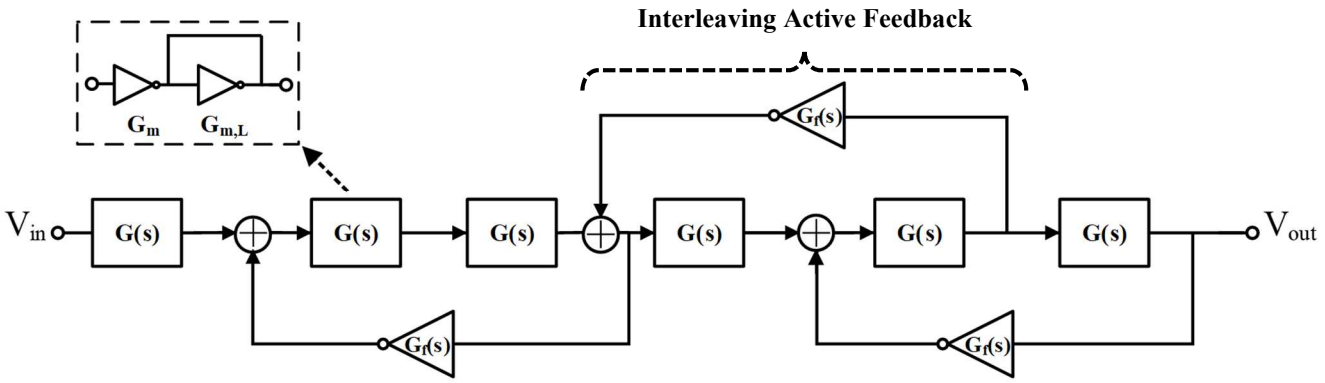

Fig. 3. Block diagram of the proposed PAM-4 linear main amplifier using g_m/g_m-based amplifiers and IAFB technique.

As mentioned in Section II, negative active feedback causes gain peaking, and IAFB reduces it. Fig. 4 shows the frequency response of the proposed design with different combinations of gains for the forward blocks ($G(s)$) and feedback inverters ($G_f(s)$) to have a total gain of 64. It can be seen that increasing the gain of the feedback inverters increases both bandwidth and gain peaking. The amount of gain peaking for the different combinations of $G(0)$ and $G_f(0)$ is demonstrated in Fig. 4. IAFB can result in significant pole-splitting if the loop gain becomes excessively large. This pole-splitting can lead to a situation where a pair of conjugate poles shifts into the right half-plane, making the system unstable. Fig. 5 illustrates the pole locations of the proposed main amplifier for different combinations of $G(s)$ and $G_f(s)$ DC gains to have a total gain of 64. This plot shows that the far-right pair of conjugate poles moves toward the right half-plane by increasing the feedback gain and the forward gain. To ensure a stable system, the poles of (3) must have negative real parts. Therefore, we must be careful in choosing the design point to avoid instability and unbounded dynamic response.

Fig. 6 shows how vertical eye-opening (VEO) changes in different combinations of $G(0)$ and $G_f(0)$. The largest VEO happens at $G(0)$=3.3 and $G_f(0)$=0.29, but as $G(0)$ and $G_f(0)$ increase, the jitter of the eye diagram gets larger. Based on all these tradeoffs, the forward and feedback gains are chosen to be $G(0)$=3 and $G_f(0)$=0.23. To compare the frequency response of the g_m/g_m-based design with and without feedback and the CH-based design, Fig. 7 is plotted. It is evident that the feedback has significantly improved the bandwidth of the g_m/g_m circuit. The ratio of 2.5 between PMOS and NMOS transistor widths is kept in all three configurations, and each CH stage is designed to have a gain of 2. At the same total gain of 64 (~36 dB), the g_m/g_m-based circuit with three negative active feedback has the widest bandwidth.

To investigate the linearity of the g_m/g_m-based design with and without feedback and the CH amplifier, the THD of these topologies is plotted in Fig. 8 for a range of input voltage. The CH amplifier has the worst linearity (highest THD) in the entire range of the input voltage. The linearity of the open-loop g_m/g_m amplifier is the best in small input voltage amplitudes while adding feedback improves linearity at higher voltages. Linear feedback usually improves linearity. However, when applied to inverter-based designs, the feedback network is nonlinear. Specifically, the feedback inverter whose input is connected to the overall output sees a very large input signal, exceeding its linear range. Its distortion cannot be easily eliminated, explaining why the IAFB design does not exhibit better linearity across all input voltages compared to the open-loop design. We also designed and simulated the fully differential configuration of the proposed design and expected to see a noticeable decrease in the THD due to the elimination of the even-order harmonics. However, the amount of the THD reduction was insignificant. A pseudo-random bit source (PRBS) is given to a conventional shunt-feedback TIA input, and the output of the TIA is connected to the proposed main amplifier. Fig. 9(a) displays the eye diagram of the circuit in the NRZ signaling scheme at $G(0)$=3 and $G_f(0)$=0.23, and Fig. 9(b) represents it in PAM-4 format with a unit interval (UI) of

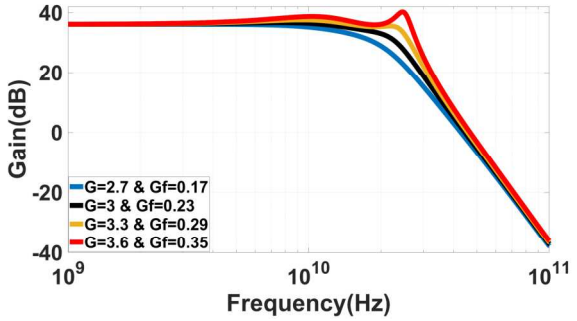

Fig. 4. Gain peaking for different combinations of $G(0)$ and $G_f(0)$ to have a total gain of 64.

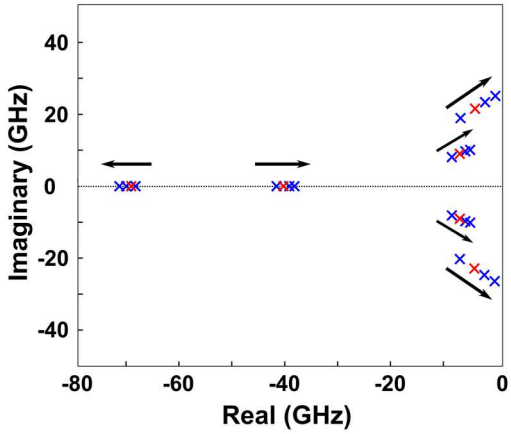

Fig. 5. Pole location variations of the proposed design for different combinations of $G(s)$ and $G_f(s)$ to have a total gain of 64. The red markers represent the pole locations of the design with $G(0)$=3 and $G_f(0)$=0.23.

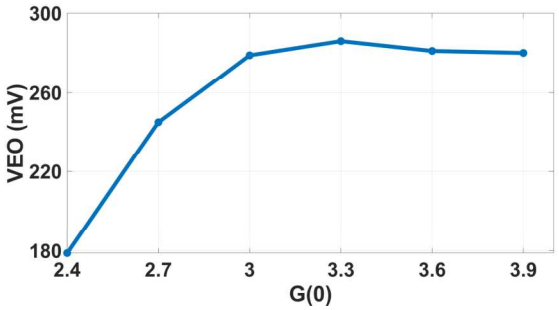

Fig. 6. VEO variations of the six-stage g_m/g_m design with IAFB in different combinations of $G(0)$ and $G_f(0)$.

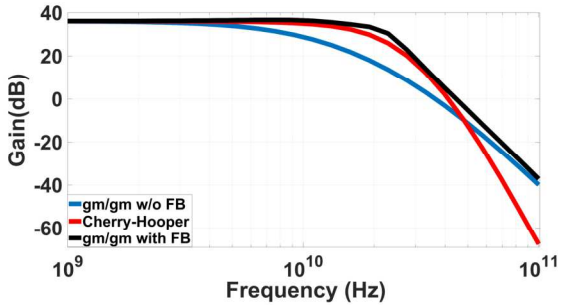

Fig. 7. Frequency response of the six-stage g_m/g_m-based design with and without IAFB at $G(0)$=3 and $G_f(0)$=0.23, and six-stage CH-based amplifier.

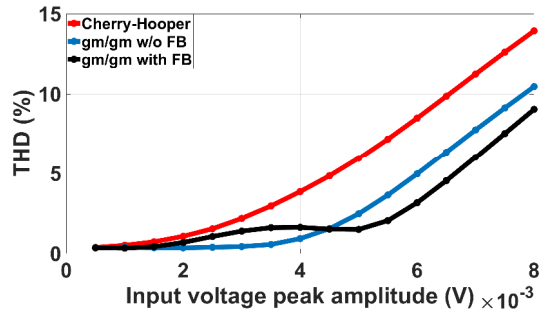

Fig. 8. THD of the six-stage g_m/g_m-based design with and without IAFB at $G(0)$=3 and $G_f(0)$=0.23, and six-stage CH-based main amplifier.

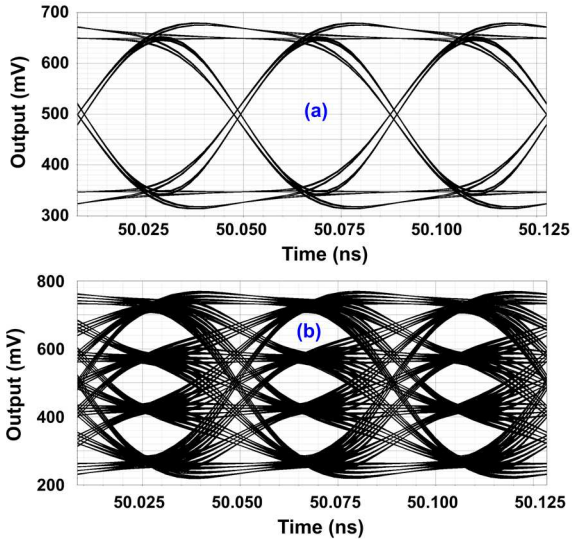

Fig. 9. The eye diagrams of the proposed design in a) NRZ, b) PAM-4 at $G(0)$=3 and $G_f(0)$=0.23 with 40 ps of UI.

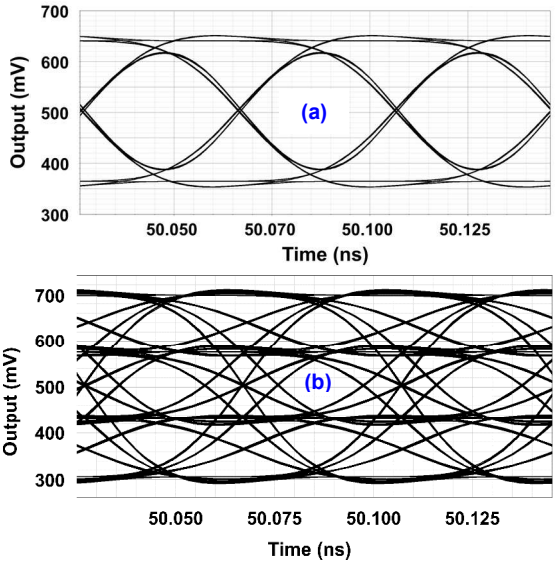

Fig. 10. The eye diagrams of the CH-based design in a) NRZ, b) PAM-4 with 40 ps of UI.

40 ps. Fig. 10(a) and (b) demonstrates the NRZ and PAM-4 eye diagrams for CH-based topology, respectively. Apart from the higher bandwidth and better linearity than the CH-based design, the proposed design also represents a larger VEO. The performance comparison summary of three simulated configurations in single-ended mode is tabulated in Table I. Table II compares the proposed design's performance with previous works in which various design techniques for bandwidth and linearity improvement are employed.

TABLE I. SIMULATION RESULTS COMPARISON SUMMARY

	CH amplifier	*Open-loop g_m/g_m-based*	*g_m/g_m-based with IAFB*
Gain (dB)	36.12	36.12	36.12
Bandwidth (GHz)	14.4	5.9	19.4
THD* **@ 1 GHz** (%)	5.96	2.48	1.5
Transimpedance gain (dBΩ)	78.1	78.1	78.1
VEO** **(TIA+amps)** (mV)	227	71.5	279
Output noise (mV_{rms})	18.65	11.34	19.7
Power consumption (mW)	18.66	12.75	11.67

* Input voltage of ± 5 mV, and the output swing of > 600 mV_{pp} ** Input current of ± 18 µA

IV. CONCLUSION

A highly linear main amplifier is proposed based on the g_m/g_m amplifier and IAFB technique for PAM-4 optical receivers with a data rate of 50 Gb/s. The proposed design's bandwidth, linearity, and VEO are compared to those of the CH amplifier. Simulation results show that the g_m/g_m-based configuration offers a wider bandwidth than the CH amplifier when applying the IAFB technique. Moreover, at the same input, the linearity and VEO of the proposed circuit are superior to the CH amplifier. To the best of the authors' knowledge, the proposed design is the first example of the IAFB-based topology using inverter-based amplifiers.

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TABLE II. PERFORMANCE COMPARISON WITH PREVIOUS WORKS

Reference	***Technology***	***BW extension/ Linearity Technique***	***Data rate (Gb/s)***	***Transimpedance Gain (dBΩ)***	***Bandwidth (GHz)***	***THD (%)***	***Result Type***
[6]	180 nm CMOS	3rd-order IAFB/ -	10 (NRZ)	42 dB*	9	NA	Measurement
[4]	16 nm FinFet	Passive inductors/ g_m/g_m amplifiers	106.25 (PAM-4)	78	27	< 2 @600 mV_{pp}	Measurement
[2]	65 nm CMOS	CH amplifiers with IAFB/ -	25 (NRZ)	69.4	13.6	NA	Measurement
[15]	130 nm SiGe BiCMOS	Negative impedance converter (NIC) CTLE/ Emitter degeneration	112 (PAM-4)	70	37~48	< 5 @600 mV_{pp}	Measurement
[16]	40 nm Bulk CMOS	CTLE/ Tunable gain	50 (PAM-4)	66	23.4	< 3 @400 mV_{pp}	Post-layout simulation
This work	65 nm CMOS	3rd-order IAFB/ g_m/g_m amplifiers	50 (PAM-4)	78.1	19.4	< 1 @600 mV_{pp}	Schematic simulation

* Gain of the main amplifier without TIA