Modeling and Validation of Offset Cancellation for Hybrid Photonic-Electronic Transimpedance Amplifier Using All-Electronic Circuits

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***Abstract*—Hybrid photonic-electronic circuits involving cross-domain feedback signals are difficult to validate and troubleshoot. This paper describes an approach to model and validate an offset-cancellation loop for a hybrid transimpedance amplifier (TIA) using all-electronic circuits. An equivalent electrical model is developed for the tunable interferometer attenuators used for offset trimming, and it includes test features to extract the system performance. The stability analysis of the system shows 75° of phase margin and 102 dB of gain margin. Measurement results demonstrate good agreement with analysis and successful TIA offset cancellation.**

***Index Terms*—Hybrid photonic-electronic circuit, transimpedance amplifier (TIA), offset-cancellation, stability analysis, equivalent circuit modeling.**

I. Introduction

Hybrid photonic-electronic circuits are widely adopted in fibre-optic communication systems [1], [2], scientific imaging instruments [3]–[6], light detection and ranging, biomedical devices [7], [8], and quantum computing [9]–[16]. Other hybrid designs are becoming increasingly common [17]–[23]. A common challenge with hybrid circuits is the difficulty in modeling and validating the system due to the complexity of the cross-domain interactions. For example, if a photonic integrated circuit (PIC) passes an optical signal into a photodiode to be amplified on an electronic integrated circuit (EIC), the testbench will require both optical and electronics test setup involving dedicated hardware and instruments as well as cross-domain expertise. This is further complicated if there is feedback across the domains, i.e. a hybrid closed-loop system. This multi-domain testing can present a large barrier to entry and challenges in isolating system issues should they arise. Therefore, it is desirable to be able to independently test and characterize each PIC and EIC before their integration. This relies on innovative ways to model and construct the cross-domain circuit in a single domain (i.e. all-electronic) such that the test setup captures the behavior of the hybrid system to offer the ability to understand, quantify, and troubleshoot the circuit. This is especially relevant in hybrid, closed-loop systems where the forward and feedback signals cross both the optical and electronic domains.

Several recent publications have utilized integrated optics and photonics, with varying approaches to testing and validation. The work in [10] consists of a custom transimpedance amplifier (TIA) and PIC, but doesn't present efforts to individually test each system. The characterization appears to make some estimations regarding the performance of the electrical system, which could lead to additional measurement error. Similarly, in [9], no attempt was presented to characterize each system individually. Instead, the work externally measures the current from the PIC into the TIA during operation. This would likely add a large capacitive load to the input of the TIA, potentially complicating interpretation of the results. Further, [9] implements a feedback loop from the EIC to tune the PIC, however no stability analysis or individual testing of this loop is described. The design in [11] uses an unpackaged commercial TIA with a custom PIC, but there is no individual TIA verification. Instead, the paper implies reliance on the packaging parasitic values from a datasheet, potentially leading to some measurement inaccuracy or even system instability. In [12], their testing is able to measure the performance of the EIC's directly, but there is no attempt to model the PIC.

In this paper, we describe an approach to model and validate a hybrid photonic-electronic offset-cancellation circuit for a transimpedance amplifier. Our proposed system models the optical side with equivalent electrical components to create an all-electronic feedback loop. The proposed technique enables the stability analysis, eliminates the need for multi-domain design (optical and electrical) of test equipment, is easily implemented with generally available lab equipment and components, and validates the closed-loop performance.

II. Circuit Design and Analysis

The hybrid photonic-electronic system (Fig. 1(a)) consists of a PIC and an EIC to amplify optical signals for quantum key distribution [24], [25] and it will be described in detail in a future publication. Briefly, the output of the PIC consists of

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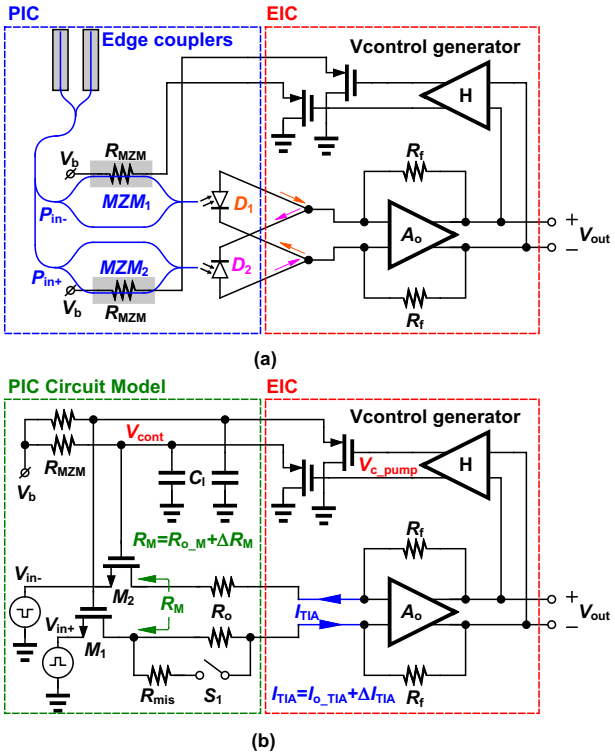

Fig. 1: (a) Schematic of hybrid photonic-electronic transimpedance amplifier with offset cancellation. Optical waveguides are drawn in blue. The PIC consists of a 2x2 MMI with 50:50 output. Each output is fed through an MZM and into a photodiode. (b) Schematic of proposed all-electronic circuits with PIC replaced with equivalent electrical components. S_1 is implemented as a push button for convenience. $R_{\text{mis}} \gg R_o$ to model realistic PIC mismatch.

two Mach-Zehnder Modulators (MZM), MZM_1 and MZM_2, which act to attenuate the optical signal. Each MZM is fed by a differential signal, $P_{\text{in}-}$ and $P_{\text{in}+}$, respectively. The MZMs drive two cross-coupled photodiodes, D_1 and D_2, which are designed so that, when balanced, the DC current generated by them is subtracted off and the TIA amplifies only the differential AC signal. However, the mismatch between the two photodiodes and optical paths due to fabrication injects a differential signal into the TIA, possibly saturating it. To cancel this offset, the feedback system, H, measures the DC voltage offset at the TIA output and tunes it out by changing the bias voltages on the MZMs. By canceling the offset on the PIC side, the dynamic range requirement for the TIA is relaxed.

It is desirable to model the PIC electronically to be able to characterize and troubleshoot the EIC and the closed-loop system. This requires a mimic circuit (Fig. 1(b)) that can perform the following functions: it needs to generate AC and DC currents matching the responsivity of the photodiodes, and it needs to respond to the control voltages by varying the AC and DC current of each input channel independently. We begin with a circuit to produce the input signals by placing two voltage sources, $V_{\text{in}+}$ and $V_{\text{in}-}$ (from an arbitrary waveform generator), in series with large resistors, R_o. The input impedance of the TIA is given by $R_f/(1+A_o)$ [26]. With an ideal op amp the input impedance of the TIA would be zero ohms and the input current would be set solely by the voltage source and series resistance. In practice, the op amp gain is finite and the input impedance is greater than zero. To reduce this effect we choose R_o to be several orders of magnitude greater than the effective input impedance of the TIA.

The feedback element needs to measure the feedback voltage and decrease the input current correspondingly. To do this we place an NMOS transistor (VN2016), (M_1 and M_2), in series with R_o and connect its gate to the control voltage. Due to the DC biasing of this NMOS it acts like a variable resistor, increasing R_{ds} (resistance from drain to source) as the gate voltage decreases. We add switch S_1 and resistor R_{mis} to model the mismatch in the PIC. The EIC is designed to accommodate a wide-range of mismatches. By turning S_1 on (or off), we vary the equivalent resistance by adding (or removing) R_{mis} in parallel with R_o. Toggling the switch generates a step input to the circuit, allowing us to check for the settling behavior and stability of the closed-loop system. We can also observe the loop settling for various pole frequencies by varying the capacitor C_l, which models the time delay produced by the MZM optical attenuators. The

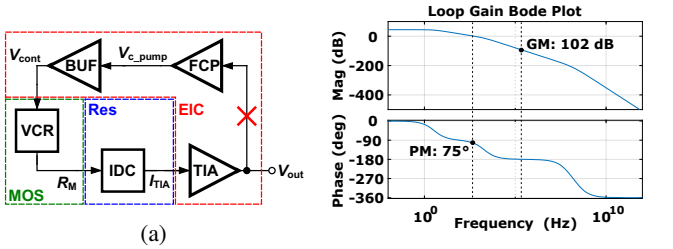

Fig. 2: (a) Block diagram of TIA offset cancellation loop using all-electronic circuits. "X" indicates loop break point for stability analysis. (b) Loop gain bode plot using typical values.

offset-cancellation negative feedback loop works to null out the offset at the output of the TIA. For stability analysis, we break the loop between the TIA output and the offset-sensing amplifier FCP which presents a high input impedance (Fig. 2(a)). The transfer function of FCP can be modeled as [27], [28]:

$$FCP(s) = \frac{V_{c\_pump}}{V_{out}} = A_{comp} I_{cp} \left(sC_{cp} + \frac{1}{R_{cp}} \right)^{-1} \quad (1)$$

We can observe that, with the PIC circuit model in place, the output of the voltage generator is buffered by a common-drain amplifier with a discrete capacitor load. The transfer function for this is presented in (2).

$$BUF(s) = \frac{V_{cont}}{V_{c\_pump}} = \frac{g_m R_{MZM}}{sC_l R_{MZM} + g_m R_{MZM} + 1} \quad (2)$$

The NMOS variable resistor in triode is nonlinear in nature. To complete our open-loop analysis we linearize the NMOS's response around three bias points, typical, worst, and best case. We consider each in our stability analysis and measurement. The NMOS operates in triode and turns a small change in gate voltage, dV_g, into a small change in the drain-to-source resistance, dR_M. To linearize this function we observe that increasing V_g, decreases R_M. By sweeping V_g, and creating a table of R_M values, we can generate a best-fit quadratic function for the NMOS response. We linearize the best-fit equation at selected voltages. From each we can extract the slope at that point and call it $-K$, the linearized dR_M/dV_g response of the NMOS. We can express this in like fashion as (3):

$$VCR(s) = \frac{dR_M}{dV_{cont}} = -K \tag{3}$$

We next analyze the effect a ΔR_M has on the input current, ΔI_{TIA}, to the TIA. We begin our analysis by considering both the initial (I_{o_TIA}) and variable (ΔI_{TIA}) input currents. We similarly consider the initial (R_{o_M}) and variable (ΔR_M) NMOS resistance. The input current can be expressed as (4):

$$I_{o\_TIA} + \Delta I_{TIA} = \frac{V_{outdc} - V_{indc}}{R_o + R_f + R_{o\_M} + \Delta R_M} \tag{4}$$

By use of the Binomial approximation and the assumption $\Delta R_M \ll R_o + R_f + R_{o\_M}$, we can rewrite (4) as:

$$I_{o\_TIA} + \Delta I_{TIA} \approx \frac{V_{outdc} - V_{indc}}{R_o + R_f + R_{o\_M}} \times \left(1 - \frac{\Delta R_M}{R_o + R_f + R_{o\_M}}\right) \tag{5}$$

The DC condition of the circuit consists of:

$$I_{o\_TIA} = \frac{V_{outdc} - V_{indc}}{R_o + R_f + R_{o\_M}} \tag{6}$$

Applying this to (5) allows us to subtract the DC condition on both sides, thus leaving only the AC response. Combining terms and rewriting yields the transfer function:

$$IDC(s) = \frac{\Delta I_{TIA}}{\Delta R_M} = \frac{V_{indc} - V_{outdc}}{(R_o + R_f + R_{o\_M})^2} \tag{7}$$

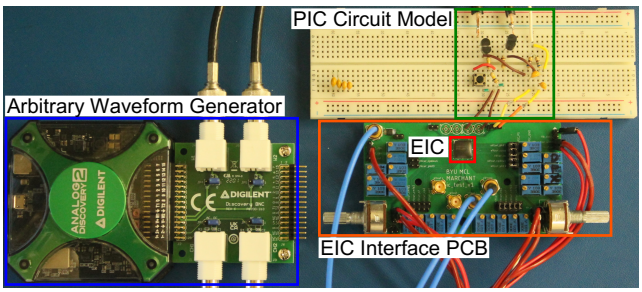

Fig. 3: Picture of physical test setup, packaged EIC, PCB interface board, and breadboarded PIC circuit model.

The transfer function of the TIA can be modeled as a two-pole system. The op amp is represented as a single-pole system with a DC gain A_o and a pole of ω_o [29]. A second pole is found at the input of the TIA. C_{in} is the capacitance on the input node. The input resistance is given by the feedback resistance R_f reduced by the gain of the op amp through the Miller effect [30]. The transfer function is given as

$$TIA(s) = \frac{V_{out}}{I_{TIA}} = \frac{A_0\omega_0}{C_{in}}\left(s^2 + s\frac{R_fC_{in} + 1/\omega_0}{R_fC_{in}/\omega_0} + \frac{(A_0+1)\omega_0}{R_fC_{in}}\right)^{-1} \tag{8}$$

Combining the transfer functions of all the above blocks yields the overall open-loop transfer function:

$$\begin{aligned} Aol(s) =& FCP \times BUF \times VCR \times IDC \times TIA \\ =& \frac{-KA_{comp}A_0\omega_0(V_{indc} - V_{outdc})}{C_{in}(R_o + R_f + R_{o\_M})^2} \\ &\times \left[s^4\left(C_{cp}C_lR_{MZM}\right) \right. \\ &+ s^3\left(C_{cp}g_mR_{MZM} + \frac{C_lR_{MZM}}{R_{cp}}\right) \\ &+ s^2\left(C_{cp} + \frac{g_mR_{MZM}}{R_{cp}} + \frac{R_fC_{in} + 1/\omega_0}{R_fC_{in}/\omega_0}\right) \\ &\left. + s\left(\frac{1}{R_{cp}} + \frac{(A_0+1)\omega_0}{R_fC_{in}}\right) + \left(\frac{(A_0+1)\omega_0}{R_fC_{in}}\right)\right]^{-1} \end{aligned} \tag{9}$$

The open-loop transfer function contains four poles, potentially leading to instability. In our design, the two poles in the TIA are 70 MHz and 500 MHz, the feedback pole is 2 kHz, and the pole introduced by the optical attenuators/PIC circuit model is on the order of a few Hz. Therefore, due to the much lower frequency of the dominant pole, the closed-loop system is stable. The specific frequency depends on the selected discrete load capacitor. With a selected C_l of 1 mF the dominant PIC circuit model pole frequency about 3.3 Hz.

Choosing typical values for the NMOS linearized resistance and the PIC model load capacitor yields a phase margin of 75° and a gain margin of 102 dB. With worst-case values, the phase margin drops to 60° and gain margin to 94 dB. Thus we verify that the closed-loop performance will be stable over a variety of operating conditions.

III. Measurement Results

Fig. 3 shows our test setup with the packaged EIC, interface PCB, and breadboarded circuit which models PIC. The input signal was generated by an arbitrary waveform generator (Digilent Analog Discovery 2). We verify the loop stability by applying a step input (ΔR) with the switch S_1 (Fig. 1(b)) as described earlier. We then break the feedback loop to observe the response at V_{cont} by measuring its rise/fall time to check against our analytical values for the dominant pole.

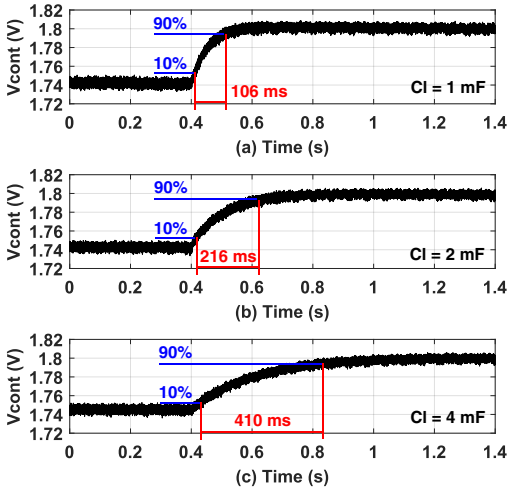

Fig. 4: Settling time of feedback loop with three different load capacitors C_l. (a) 3.3 Hz at 1 mF. (b) 1.6 Hz at 2 mF. (c) 0.85 Hz at 4 mF. The corner frequency f_c is derived from the 10% to 90% rise time by calculating the RC time constant: $\tau = \Delta t/ln(9)$, which gives $f_c = 1/(2\pi \times \tau)$.

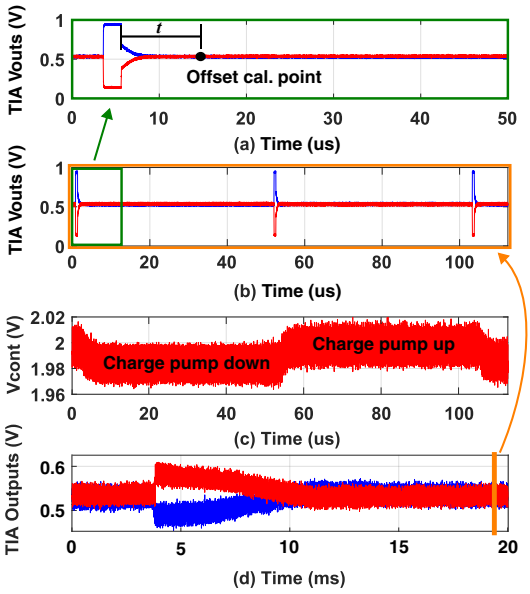

Fig. 5: (a) Expanded view of TIA output data sync pulses. The offset calibration point is where the offset is measured from by the feedback circuit. (b) TIA output showing data sync pulses and aligned DC levels. (c) Settled control voltages showing approximately trapezoidal waveform from charge pumping. (d) TIA output settling from step input resistance mismatch ΔR_M. Data sync pulses are removed for clarity. Note: TIA output noise is greater than typical likely due to environmental noise sources, EMI.

Fig. 4 shows the rise time of the control voltages with three different capacitive loads. C_l values of 1 mF, 2 mF, and 4 mF, yield corner frequencies of 3.3 Hz, 1.6 Hz, and 0.85 Hz, respectively. This matches the anticipated corner frequency of the dominant pole as suggested by the open-loop transfer function, validating our analysis.

Fig. 5 shows the closed-loop TIA outputs and feedback control voltages. The feedback circuitry senses the offset at some point t μs after the falling edge of the data sync pulse. We can see the control voltage pump up or down at this time, and then hold until the next data cycle. In its settled state the control voltages will have a small trapezoidal waveform based on the parameters of the feedback circuit. Fig. 5(d) shows the loop settling given the step input. The step is applied by activating the switch S_1 to reduce the series resistance of one side of the differential input to the TIA. This induced mismatch creates an offset at the output. It is quickly minimized as the feedback loop restabilizes at a new control voltage level. We conclude that the feedback loop has sufficiently high phase and gain margin as we observe no oscillations or ringing in the loop response as predicted by our analysis. The closed-loop bandwidth is measured to be 78 Hz and is sufficient to track offset drifts due to environmental changes which are slow moving.

By modeling the range of the expected parameters from the PIC, we have been able to verify the performance of the TIA and offset-cancellation loop. With good agreement between the theoretical and measured performance, we have validated the use of an electrical circuit model for the PIC in preparation to integrate the electronic and optical systems as a hybrid system.

TABLE I: Performance Summary

	Typical	Minimum
OL DC Gain	52 dB	49 dB
OL BW$_{-3dB}$	3.2 Hz	0.81 Hz*
Phase Margin	75°	60°
Gain Margin	102 dB	94 dB
OL Settling Time	106 ms	410 ms
EIC Power	102 mW	-
PIC Buffer Power	20 mW	-
PCB Power	76 mW	-
Technology	180 nm + Discrete	-

*Lower f_c possible with larger load capacitor.

IV. Conclusion

This paper presents a technique to model and validate an offset-cancellation loop of a hybrid transimpedance amplifier using all-electronic circuits. The equivalent electrical circuit mimics the characteristics of the tunable interferometer attenuators for offset trimming, and provides means to analyze the dynamics and stability of the feedback loop. Due to the modular nature of the discrete circuit, it is possible to validate a wide range of PIC performance metrics. Further, the system easily allows for iterative testing between fully-integrated and all-electronic testing. If the PIC performs outside of expected bounds, the EIC can still easily be tested and tuned in a controlled environment to perform in these edge cases. The system exhibits 75° of phase margin and 102 dB of gain margin with typical conditions. Measurement results show good agreement with analysis and successful TIA offset cancellation.

REFERENCES

[1] D. Li, G. Minoia, M. Repossi, D. Baldi, A. Ghilioni, E. Temporiti, and F. Svelto, "A 25gb/s 3d-integrated silicon photonics receiver in 65nm cmos and pic25g for 100gbe optical links," in *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2016, pp. 2334–2337.

[2] A. Boyogueno, B. Kaminska, and M. Slamani, "A preamplifier ic design for photonic links," in *2000 IEEE International Symposium on Circuits and Systems (ISCAS)*, vol. 5, 2000, pp. 285–288 vol.5.

[3] H. Yuan, D. Zhu, X. Hu, C. Zhang, H. Xiao, and S. Pan, "Photonics-enabled biorthogonal hartley architecture for image-reject mixer with high image rejection ratio," in *2022 Cross Strait Radio Science Wireless Technology Conference (CSRSWTC)*, 2022, pp. 1–3.

[4] S. G. Stanciu, D. Coltuc, R. Hristu, C. Stoichita, and G. A. Stanciu, "Image fusion for photonic quantum ring laser structures investigated by confocal scanning laser microscopy," in *2009 3rd ICTON Mediterranean Winter Conference (ICTON-MW)*, 2009, pp. 1–4.

[5] A. Daryoush, K. Pourrezaei, K. Izzetoglu, E. Papazoglou, L. Zubkov, and B. Onaral, "Microwave photonics applied to fnir based biomedical imaging?" in *2009 IEEE LEOS Annual Meeting Conference Proceedings*, 2009, pp. 729–730.

[6] D. Geuzebroek, A. van Rees, E. Klein, and K. Lawniczuk, "Ultra-wide band (400-1700nm) integrated spectrometer based on arrayed waveguide gratings for spectral tissue sensing," in *2017 IEEE 14th International Conference on Group IV Photonics (GFP)*, 2017, pp. 83–84.

[7] I. Mohammad, V. Rymanov, S. Makhlouf, I. Stoffels, J. Klode, X. Tang, M. Ali, and A. Stöhr, "Photonic non-invasive mmw and thz imaging for non-melanoma skin cancer detection," in *2022 Fifth International Workshop on Mobile Terahertz Systems (IWMTS)*, 2022, pp. 1–5.

[8] N. Peserico, A. Annoni, A. Varriale, S. D'Auria, L. Bellieres, F. Cuesta-Soto, M. Rodrigo, S. Peransi, and A. Melloni, "Experimental demonstration of integrated photonic free-label biosensor for cbrn threats using micro-ring resonators," in *2016 18th International Conference on Transparent Optical Networks (ICTON)*, 2016, pp. 1–4.

[9] C. Bruynsteen, M. Vanhoecke, J. Bauwelinck, and X. Yin, "Integrated balanced homodyne photonic–electronic detector for beyond 20 ghz shot-noise-limited measurements," *Optica*, vol. 8, no. 9, pp. 1146–1152, 2021.

[10] F. Raffaelli, G. Ferranti, D. H. Mahler, P. Sibson, J. E. Kennard, A. Santamato, G. Sinclair, D. Bonneau, M. G. Thompson, and J. C. F. Matthews, "A homodyne detector integrated onto a photonic chip for measuring quantum states and generating random numbers," *Quantum Science and Technology*, vol. 3, no. 2, p. 025003, 2018.

[11] J. F. Tasker, J. Frazer, G. Ferranti, E. J. Allen, L. F. Brunel, S. Tanzilli, V. D'Auria, and J. C. F. Matthews, "Silicon photonics interfaced with integrated electronics for 9 ghz measurement of squeezed light," *Nature Photonics*, vol. 15, pp. 11–15, 2021.

[12] C.-X. Zhu, Z.-Y. Chen, Y. Li, X.-Z. Wang, C.-Z. Wang, Y.-L. Zhu, F.-T. Liang, W.-Q. Cai, G. Jin, S.-K. Liao, and C.-Z. Peng, "Experimental quantum key distribution with integrated silicon photonics and electronics," *Physical Review Applied*, vol. 17, p. 064034, 2022.

[13] J. W. Silverstone, L. M. Rosenfeld, D. A. Sulway, B. D. J. Sayers, J. Biele, G. F. Sinclair, D. Sahin, L. Kling, J. C. F. Matthews, M. G. Thompson, and J. G. Rarity, "Silicon quantum photonics in the short-wave infrared: A new platform for big quantum optics," in *2019 Conference on Lasers and Electro-Optics Europe European Quantum Electronics Conference (CLEO/Europe-EQEC)*, 2019, pp. 1–1.

[14] H. Mahmudlu, R. Haldar, R. Johanning, A. K. Kashi, A. van Rees, J. P. Epping, K.-J. Boller, and M. Kues, "Fully on-chip laser-integrated quantum source of entangled photon states," in *2023 Conference on Lasers and Electro-Optics Europe European Quantum Electronics Conference (CLEO/Europe-EQEC)*, 2023, pp. 1–1.

[15] Y. Liu, Z. Qiu, X. Ji, A. Lukashchuk, J. He, J. Riemensberger, M. Hafermann, R. N. Wang, J. Liu, C. Ronning, and T. J. Kippenberg, "A photonic integrated circuit-based erbium-doped waveguide amplifier," in *2023 Conference on Lasers and Electro-Optics Europe European Quantum Electronics Conference (CLEO/Europe-EQEC)*, 2023, pp. 1–1.

[16] A. W. Elshaari, I. E. Zadeh, A. Fognini, D. Dalacu, P. J. Poole, M. E. Reimer, V. Zwiller, and K. D. Jöns, "Hybrid quantum photonic integrated circuits," in *2018 International Conference Laser Optics (ICLO)*, 2018, pp. 439–439.

[17] V. Kumar, S. Mishra, and V. Saxena, "Power linear dacs (pldacs) for configuration and control of silicon photonic integrated circuits," in *2023 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2023, pp. 1–5.

[18] S. Mishra, M. J. Shawon, A. Dorzhigulov, and V. Saxena, "A hybrid cmos photonic 25gbps microring transmitter with a -0.5–1.2v direct-coupled drive," in *2022 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2022, pp. 1000–1004.

[19] C. Pala, L. Thylen, M. Mokhtari, and U. Westergren, "A high-speed electro-optical analog-to-digital converter principle," in *ISCAS 2001. The 2001 IEEE International Symposium on Circuits and Systems (Cat. No.01CH37196)*, vol. 1, 2001, pp. 432–435 vol. 1.

[20] P. Ji, J. Gao, W. Xu, Y. Sun, W. He, and H. Wu, "Electronic-photonic integrated circuit design and crosstalk modeling for a high density multi-lane mzm array," in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2018, pp. 1–5.

[21] M. Shehata, M. S. Said, and H. Mostafa, "A single-wavelength photonic network on chip design based on optical orthogonal codes," in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2018, pp. 1–4.

[22] Y. Wang and T. Nguyen, "Photonic allpass filter: A versatile building block for all-optical signal processing," in *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2017, pp. 1–4.

[23] B. Radi, M. S. Nezami, O. Liboiron-Ladouceur, M. Ménard, and F. Nabki, "A 12.5 gb/s 1.93 pj/bit optical receiver exploiting silicon photonic delay lines for clock phases generation replacement," in *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2020, pp. 1–1.

[24] D. B. S. Soh, C. Brif, P. J. Coles, N. Lütkenhaus, R. M. Camacho, J. Urayama, and M. Sarovar, "Self-referenced continuous-variable quantum key distribution protocol," *Physical Review X*, vol. 5, no. 4, oct 2015. [Online]. Available: https://doi.org/10.1103/physrevx.5.041010

[25] B. Qi, P. Lougovski, R. Pooser, W. Grice, and M. Bobrek, "Generating the local oscillator "locally" in continuous-variable quantum key distribution based on coherent detection," 2015.

[26] B. Razavi, "The transimpedance amplifier [a circuit for all seasons]," *IEEE Solid-State Circuits Magazine*, pp. 10–13, 97, Winter 2019.

[27] ——, *RF Microelectronics*, 2nd ed., ser. Prentice Hall Communications Engineering and Emerging Technologies. Pearson, September 22 2011.

[28] Y. Song, S. Smith, B. Karlinsey, A. R. Hawkins, and S.-H. W. Chiang, "The digital-assisted charge amplifier: A digital-based approach to charge amplification," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 69, no. 8, pp. 3114–3123, 2022.

[29] B. Razavi, *Design of Integrated Circuits for Optical Communications, Second Edition*, 2nd ed. Wiley, August 2012.

[30] ——, *Design of Analog CMOS Integrated Circuits*, 2nd ed. McGraw Hill, January 20 2016.