SAR-MemPipe: A Hybrid Pipeline-SAR Memristive ADC for Analog Resistive Arrays

Hao You[1], Jianxiong Xu[1], Amirali Amirsoleimani[2], Mostafa Rahimi Azghadi[3], and Roman Genov[1]
[1]*Department of Electrical and Computer Engineering*, University of Toronto, Toronto, Canada
[2]*Department of Electrical Engineering and Computer Science*, York University, Toronto ON M3J 1P3, Canada
[3]*College of Science and Engineering*, James Cook University, Townsville, Australia
hao.you@mail.utoronto.ca, roman@eecg.utoronto.ca

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***Abstract*—This paper presents a hybrid pipeline SAR ADC with a loop-unrolled structure to reduce the crossbar's ADC power while maintaining high speed. The 1^{st} stage memristive SAR ADC can fully utilize the TIA originally in the crossbar and avoid the extra MDAC in pipeline ADC. Further, memristive weight calibration and a new resistive alternated binary search are implemented on the 1^{st} stage to maintain the TIA gain and ADC's accuracy. Both stage's ADC are loop-unroll to eliminate the delay brought by SAR logic for high speed. Through multiple simulations, the design is demonstrated to be robust to the frequency and mismatch variations with the highest sampling frequency reaching 300MHz and SNDR up to 65.1dB in 9MHz input. The power consumption is designed to be as low as 6.7mW, which helps the ADC to achieve a 15.2fJ/conv FoM. Not limited to the crossbar, the presented ADC also shows promising potential for applications in various fields (biomedical, IoT etc.) for general purposes.**

***Index Terms*—Pipeline SAR ADC, loop-unrolled SAR, resistive SAR, Memristor**

I. Introduction

With the convenience brought by machine learning (ML), the computing architecture has evolved at the same time to fulfill the tremendous computing requirements of more and more complex algorithms. While vector-matrix multiplication (VMM) has taken most parts of neural network computing, in-memory computing with resistive crossbar architecture is developed to facilitate the efficiency of multiply and accumulate (MAC) operation in VMM [1]–[3].

Fig. 1(a) shows a classic resistive crossbar architecture [3]. After digital input is converted to analog voltage through digital to analog converter (DAC), the input voltage is multiplied by the conductance (G_i) of resistive memory. The transimpedance amplifier (TIA) then sums the currents on the line to an analog voltage that analog to digital converter (ADC) will convert to digital output. Though these circuits are critical components in the resistive crossbar, the ADC can take up to 58% of total power and 31% of total area [4]. Thus, a highly consumption-efficient ADC with adequate accuracy is necessary. A widely used ADC in the resistive crossbar is SAR-ADC. It has the advantage of low power and area compared to the flash ADC as the resolution increases. However, SAR has a linear increase in latency due to its binary search mechanism which largely decreases the crossbar throughput [5]. As mentioned in [6], latency by SAR logic can take up to 75% of total delay. One potential solution is to eliminate the latency by SAR logic between each bit calculation by the loop-unroll structure as shown in Fig. 1(b)

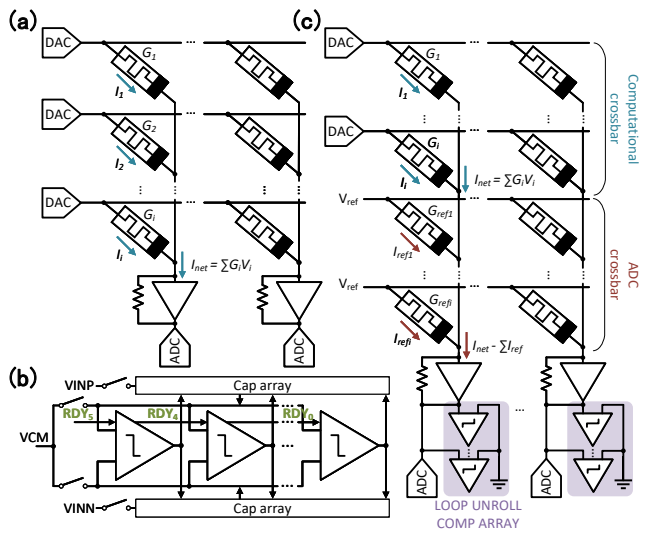

Fig. 1. (a) A classic resistive in-memory computing crossbar. (b) The architecture of loop-unrolled cap SAR-ADC. (c) The general structure of the proposed ADC.

[7]. With the help of appending a comparator to each bit determination, the next bit can be compared directly from the previous comparator result without SAR logic.

To further improve the throughput, the proposed 13-bit ADC will adopt the pipeline structure that parallels two loop-unroll SAR ADC. Besides that, to avoid extra power and area-consuming MDAC, the TIA in the crossbar is reused for the pipeline subtractor, and the trainable memristive weight is applied for the 1^{st} stage ADC to increase accuracy and adapt with the TIA subtractor. With the training mechanism, the memristive weight in 1^{st} stage ADC can be flexibly used either for crossbar computation or ADC quantization.

The rest of the paper will first describe the circuit mechanism, implementation, and working process. Then we will introduce the training (calibration) mechanism in the memristive SAR-ADC. Finally, we will discuss the simulation results based on various evaluation indexes.

II. Circuit Mechanism

Fig. 1(c) shows the general structure of the proposed ADC. The 1^{st} stage is a 6-bit memristive SAR ADC that roughly quantizes the analog current output from the computing crossbar. The residual voltage after TIA subtraction will be transferred to 2^{nd} stage 7-bit cap SAR-ADC for fine quantization.

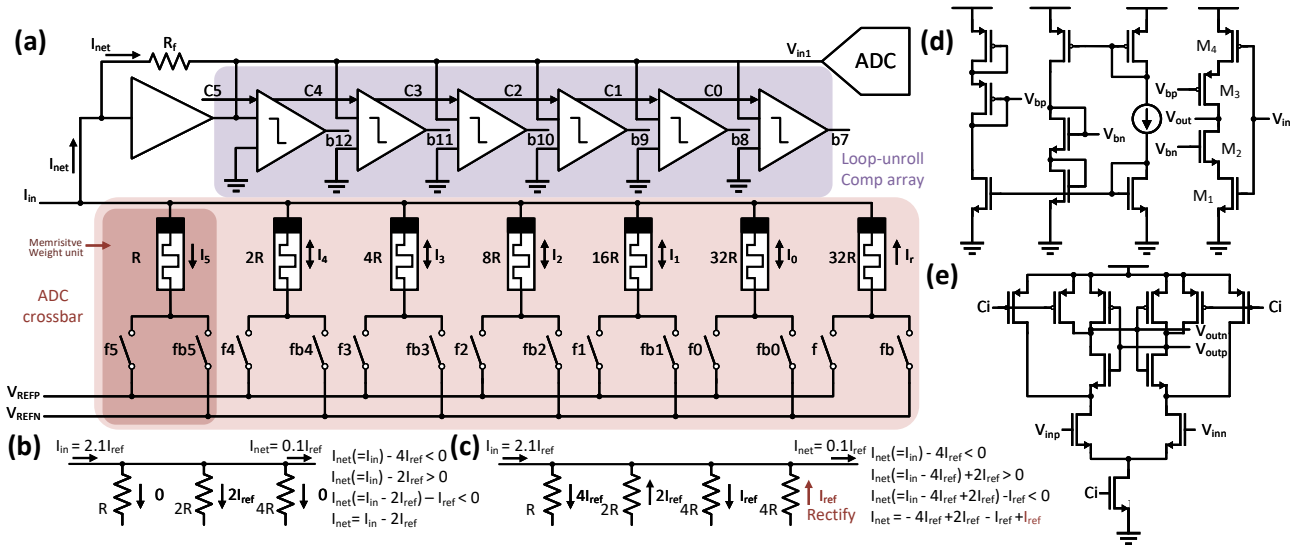

Fig. 2. (a) The circuit implementation of the 1^{st} stage memristive SAR ADC. (b) The traditional current withdraws resistive binary search implementation. (c) The proposed alternative resistive binary search implementation. Current flow through all resistors at all times. (d) The cascode inverter amplifier used for TIA in (a). (e) The strongARM latch comparator used in the proposed ADC.

Both ADCs adopt loop-unrolled structures to reduce the SAR logic delay.

A. Memristive SAR ADC with new binary search

Fig. 2(a) shows the 6-bit memristive SAR-ADC applied in the 1^{st} stage. A new alternative binary search implementation is applied in this ADC. As Fig. 2(b) shows, in traditional resistive binary search [8], I_{in} is compared with every reference current $2^i I_{ref}$ and as long as current I_{net} is larger than current $2^i I_{ref}$, current $2^i I_{ref}$ is minus from I_{net}. Otherwise, no current will flow through that reference current's resistor.

The problem in this implementation is the amplifier on the end cannot always see the same resistance on the left. Take Fig. 2(d), cascode inverter, as an example. Assumed the pmos side has relatively the same gain as nmos side, the loop gain (L) of the amplifier can be written as,

$$L = \frac{g_{m2}^2 r_{o1} r_{o2} (R_{in} // R_{ADC})}{R_f + R_{in} // R_{ADC} + g_{m2}^2 r_{o1} r_{o2}} \tag{1}$$

where R_{in} is the resistance from the computational crossbar, R_{ADC} is the parallel of computational resistance in ADC that has current flow through, and R_f is the feedback resistor in Fig. 1(a). While $A_{L\infty}$, the closed-loop gain when $L \to \infty$, is

$$A_{L\infty} = -\frac{R_f}{R_{in} // R_{ADC}} \tag{2}$$

The closed-looped gain (A_{CL}) can be written as,

$$A_{CL} = \frac{g_{m2}^2 r_{o1} r_{o2} R_f}{R_f + R_{in} // R_{ADC} + g_{m2}^2 r_{o1} r_{o2}} \tag{3}$$

Since R_{ADC} is the parallel of computational resistors and each computational resistor can have a greatly varied resistance, especially the most significant bit will have very small resistance, the TIA A_{CL} can vary large if the amplifier open-loop gain ($g_{m2}^2 r_{o1} r_{o2}$) is not high enough. Thus, even though the theoretical I_{net} is the same, the output of the TIA will not maintain the same with different combinations of computational resistors and cause inaccuracy on 2^{nd} stage ADC. The new binary search in Fig. 2(c) can improve this situation. The current in each resistance is bidirectional. When I_{net} is smaller than the previous $2^{i+1} * I_{ref}$, rather than cancel the previous reference current, we add a current $2^i * I_{ref}$. Utilized the property of binary that $2^i = 2^{i+1} - 2^i$, I_{net} is still minus from $2^i * I_{ref}$. And if $I_{net} > 0$, meaning the I_{net} larger than the previous reference current, the ADC will maintain the same as the traditional that withdraws $2^i * I_{ref}$ from I_{net} to have the comparison. This new binary search mechanism will make all resistors always have current flow through and let TIA see the same R_{ADC} on the left all the time. The largest bit's computational resistor always withdraws current from the input to leave space for the rest of the computational resistor to fill the current back and make sure there is always current flow through them. An extra last bit's computational resistor is added at the end to rectify the result in case the previous ΣI_{ref} makes I_{net} negative. Though it is not always connected, its resistance will be high (same as LSB reference resistance) which will not have a great influence on R_{ADC}. Fig. 2(b) and Fig. 2(c) show an example of quantization of the same I_{in} by two different resistive binary search implementations.

To fulfill the speed requirement, a single-stage cascode inverter is applied for TIA as shown in Fig. 2(d). Though its open-loop gain is limited, the closed-loop gain can be maintained stable through the new binary search mechanism above. The strong-ARM latched comparator is used for the circuit as shown in Fig. 2(e) to shorten the latch time [9].

B. Loop-unrolled SAR ADC

Fig. 3(a) shows the circuit of 2^{nd} stage loop-unrolled cap SAR-ADC. For traditional SAR-ADC with a single comparator, each bit determination cycle has the critical path

$$T_{bit} = t_{cap} + t_{latch} + t_{logic} \tag{4}$$

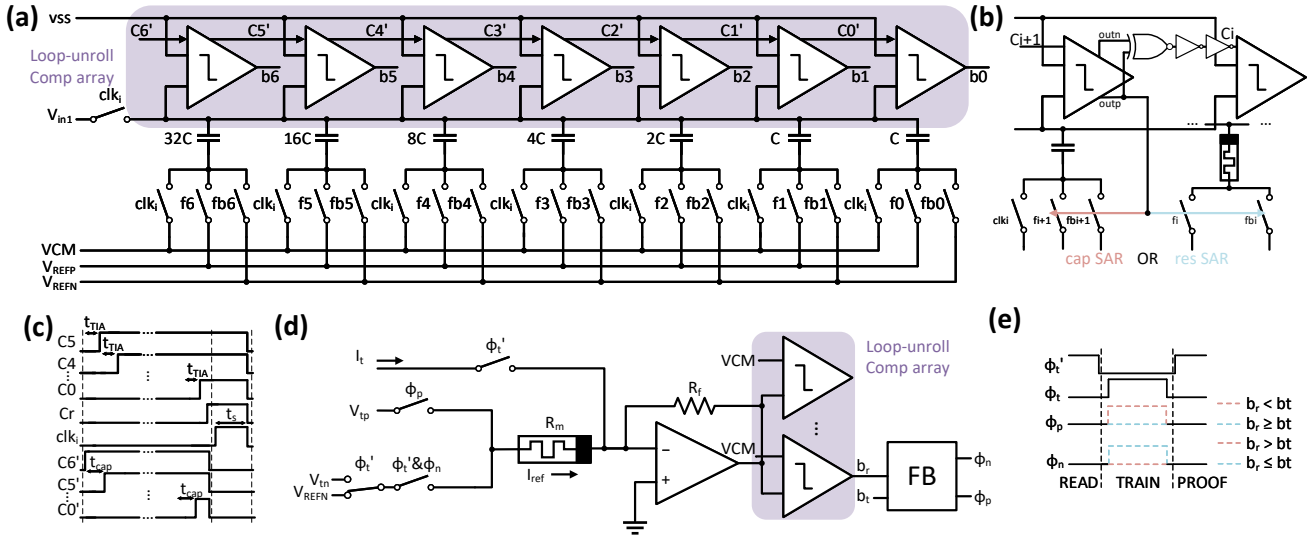

Fig. 3. (a) The circuit implementation of the 2^{nd} stage cap SAR ADC. (b) A detailed look at the loop-unroll structure. (c) The timing diagram of the proposed ADC. (d) The training circuit to calibrate the memristive weight. (e) The timing diagram of training memristive weight.

where t_{cap} is the DAC cap's settling time, t_{latch} is the comparator response time, and the t_{logic} is the time required for SAR logic [7]. As mentioned in [4], t_{logic} can consume up to 75% of total T_{bit}. To eliminate this logic delay, we can employ the loop-unrolled structure by using a comparator for each bit's determination [7]. Both purple regions in Fig. 2(a) and Fig. 3(a) are loop-unrolled comparator arrays. A detailed structure between comparators is shown in Fig. 3(b). The comparator clock now is directly from the last comparator. The previous bit result can be implemented to the corresponding switch with simple logic. With this architecture, the critical path for each bit determination can be shortened to

$$T_{bit} = t_{cap} + t_{latch} \tag{5}$$

While the 2^{nd} stage ADC is connected to multiple comparators, the captive load on the input of the comparator can be high and increase t_{latch}. To further reduce t_{latch}, the maximum DAC capacitor size is limited to 320fF with the switch having an ON-resistance of 100Ω.

Fig. 2(c) shows the timing diagram of the proposed ADC. C5 to C0 is the comparator clock of 1^{st} stage ADC. It will first wait t_{TIA} for the TIA to settle down, and compare the result. After a short t_{latch}, the result is sent back to switch for the next bit. After all 6 bits' determination, Cr is raised to check if V_{in1} needs to rectify. clki then sample the residual output V_{in1} from the 1^{st} stage to the 2^{nd} stage. C5' to C0' is the comparator clock of 2^{nd} stage ADC. The timing diagram is the same as 1^{st} stage except 2^{nd} stage compares the result first and then waits for t_{cap} for the capacitor to settle down.

III. Weight Training (Calibration)

The resistance mismatch is the key to determining the accuracy of resistive ADC [10]. We hence chose the memristor, a non-volatile passive device with changeable resistance, as the calibrable device. The memristor resistance will change when the voltage on two sides exceeds V_{on} or below V_{off} while it maintains stable otherwise [11].

In order to achieve high accuracy, the proposed ADC utilizes 2T1R memristive weight as the computational resistor [8], [12]. Fig. 2(a) dark red portion shows a unit of 2T1R memristive weight, with 2 switches and 1 memristor. Fig. 2(d)&(e) shows the training circuit and timing diagram for memristive weight. The calibration process starts by reading the current state. Memrisitor R_m is connected to V_{REFN} on the left as the normal working mode to generate corresponding I_{ref}. The training current I_t will subtract I_{ref} by TIA to get the result b_r after the comparator. The feedback will compare the b_r and b_t (the desired value) to feedback a proper signal. If $b_r < b_t$, meaning too much I_{ref} is subtracted, the feedback makes R_m connected to V_{tp} to increase the resistance of R_m by one unit. After training, the I_{ref} is reread to check if the value is correct or not. If not, the training will continue until the proof-read accepts a correct value.

With the flexibility that the memristive weight can be trained to the desired resistance, the ADC crossbar can be either used for ADC quantization or as memory units for normal crossbar computation when the accuracy requirement is not high.

IV. Evaluation

The proposed design is implemented with 65nm MOSFET technology and simulated in schematic. The memristor is simulated by the VTEAM model [13] with the physical model in [14]. Table I shows the design's details, and Table II show the comparison with the existing pipeline SAR ADC is shown in .

With the loop-unroll architecture, and high-speed comparator and amplifier, the proposed ADC is able to achieve a sampling frequency up to 300MHz. Further, the ADC's power consumption is able to reduce to 6.7mW in total, with 3.75mW consumed by cascode amplifier, 2.76mW by all comparators, 150μW by feedback resistor R_f in TIA, and 18μW by memristor in 1^{st} stage ADC. The capacitor power is under nW and hence negligible.

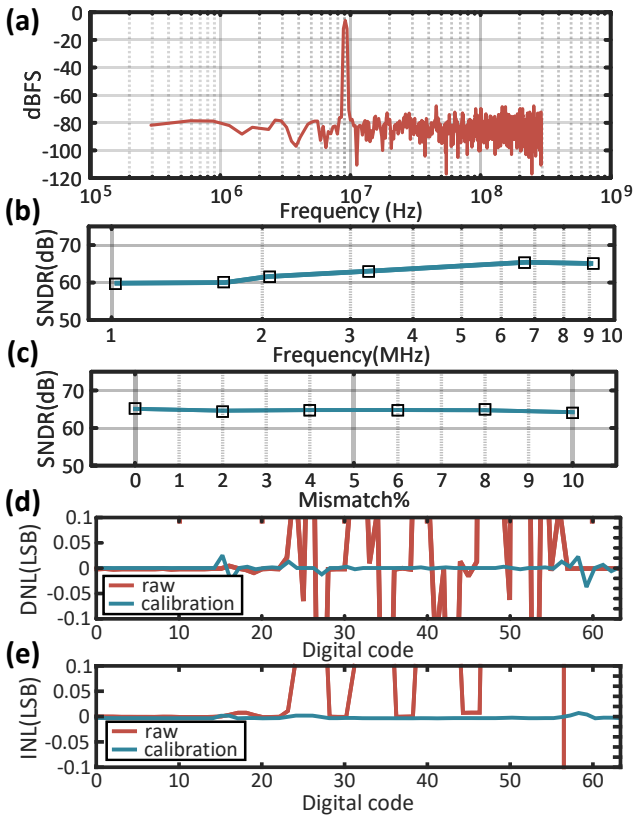

Fig. 4. (a) The output spectrum of proposed ADC at 9MHz input frequency (b)&(c) The frequency response and the mismatch test of the proposed design. (d)&(e) The DNL and INL of the 1^{st} stage ADC before calibration and after.

The calibration of memristor resistance improves the accuracy of the design. The proposed ADC's SNDR is 51dB before calibration at 9MHz input frequency and can reach 65.1dB after training the memristive weight, with the spectrum illustrated in Fig. 4(a). The DNL of the 1^{st} stage ADC reduced from 2.85/-1.5 LSB to 0.015/-0.024 LSB after calibration while INL is reduced from 6.7/-3 LSB to 0.015/-0.001 LSB as shown in Fig. 4(d)&(e). Further, the design shows great resilience to device mismatch. As demonstrated in Fig. 4(b), the ADC's SNDR can maintain around 64dB even with a high mismatch in computational capacitors. The frequency response, shown in Fig. 4(c), reveals stability across frequencies, and the SNDR can maintain over 60 dB. Combined with the advantages of speed, power, and accuracy, the proposed ADC can reach a Figure of Merit (FoM) of 15.2fJ/conv.

V. Conclusion

In conclusion, this paper introduced a new hybrid pipeline SAR ADC architecture adapted for resistive crossbar computation. The memristive SAR ADC in the 1^{st} stage hybrids perfectly with the original TIA in the resistive crossbar, reducing the extra required MDAC if the architecture is fully cap. The calibratable memristive weight is introduced on the 1^{st} stage to counter the mismatch in the amplifier and the comparator. The new alternative resistive binary search implementation stabilizes the amplifier's loop gain. This increases the ADC accuracy by maintaining the TIA output to be the same for the same residual value by TIA subtraction.

Moreover, the loop-unrolled structure with comparators array eliminates the delay from SAR logic. This reduces the cycle time for each bit calculation and helps the proposed ADC reach a high sampling speed.

With multiple simulations, the proposed ADC shows robustness on both frequency and mismatch with crossbar current input. In general, the proposed ADC would be feasible for any steady resistance current input and future work will explore more applications of the design in various fields.

TABLE I
Circuit Parameter

Circuit part	Type	Parameter	Value
1^{st} stage ADC	Transistor tech		65nm
	Sampling frequency	f_s	300MHz
	Input current range	I_{in}	0 - 120μA
	Reference voltage	$V_{REFP/N}$	1.4/1.1V
	Memristor[14]	$V_{on/off}$	0.3/-0.4V
		$R_{on/off}$	2k/100kΩ
		$k_{on/off}$	-4.8/2.8mm/s
		$\alpha_{on/off}$	3/1
	Calibration voltage	V_{tp}/V_{tn}	1.7/0.8V
	Precision		6 bits
2^{nd} stage ADC	Capacitor	C_{max}	320fF
	Common-mode	VCM	1.25V
	Reference voltage	$V_{REFP/N}$	30mV/0V
	Sampling time	t_s	0.42ns
Amplifier	Step response	t_{TIA}	0.35ns
	feedback resistor	R_f	40$k\Omega$
	Source voltage	VDD	2.5V
	Power	P_A	3.75mW
	Gain	A	30dB
Comparator	Source voltage	VDD	2.5V
	Power	P_{comp}	5μW
	Step response	t_{latch}	50ps

TABLE II
Comparison with existing SAR-ADC

	This work	[7]	[15]	[16]	[17]	[18]
Input	Current	Voltage	Voltage	Voltage	Voltage	Voltage
CMOS Node (nm)	65	65	16	65	65	40
$f_s(Hz)$	300M	300M	300M	160M	330M	160M
Power (mW)	6.7	12.5	3.6	11.1	6.23	4.96
Resolutions(bits)	13	12	12	13	12	12
SNDR(dB)	65.1	63.55	69.18	68.3	67.7	65.3
$FoM_w(fJ/conv)$	15.2	34	5.1	32.6	15.4	20.6
Calibration?	Yes	Yes	Yes	No	Yes	Yes

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