Energy Efficient Voltage-Mode Simultaneous Bidirectional Transceiver for Serial Links

Ankit Yadav[‡], V. K. Surya[‡], Sree Kumar R. G.[§], Bibhu Datta Sahoo[†], and Nijwm Wary[‡]
[‡] IIT Bhubaneswar, Bhubaneswar, India. e-mail: nijwmwary@iitbbs.ac.in
[§] Independent Researcher., Chicago, IL. e-mail: sree.analogguy@gmail.com
[†]Dept. of Electrical Eng., University at Buffalo, Buffalo, NY, USA. e-mail: bibhu@buffalo.edu

2025 IEEE International Symposium on Circuits and Systems (ISCAS) | 979-8-3503-5683-0/25/$31.00 ©2025 IEEE | DOI: 10.1109/ISCAS56072.2025.11043871

***Abstract*—This paper presents a single-ended voltage-mode (VM) simultaneous bidirectional (SBD) transceiver for chip-to-chip interconnects. A hybrid network in the receive path cancels the transmitted signal to extract the received signal enabling SBD signaling. The conventional source-series terminated (SST) and trans-impedance amplifier (TIA)-based transmitters used in the SBD signaling transceivers consume high power to minimize output impedance variation. The proposed design minimize this variation with low power consumption, thereby leading to a low-power transceiver. In addition, the power consumption while incorporating feed-forward equalizer (FFE) is reduced by using current-mode implementation in the proposed transceiver. Implemented using TSMC PDK in 65 nm technology, the simulation results gives an energy efficiency of 0.35 pJ/b at 20 Gb/s SBD data-rate.**

***Index Terms*—Voltage-mode signaling, bidirectional transceiver, serial links, Trans-impedance amplifier (TIA).**

I. Introduction

Advancements in semiconductor technology facilitate the integration of large systems on chip (SoC), leading to an increased demand for high bandwidth per I/O. However, the low-pass characteristics of the channel restrict bandwidth, necessitating power-hungry equalizers to address inter-symbol interference (ISI). The use of voltage mode transmission instead of current mode transmission reduces power consumption. Additionally, single-ended SBD signaling lowers the Nyquist frequency, thereby decreasing the power consumption of the equalizer [1]–[9].

The voltage mode transmitter-based SBD signaling transceiver, as illustrated in Fig. 1, utilizes a hybrid architecture to separate the inbound signal by subtracting the outbound signal from a replica signal on the channel. However, the challenge in this separation requires proper matching of the transmitter and replica drivers along with their corresponding loads. The mismatch between loads is exacerbated by the variation in termination in the transmitter with respect to the channel signal [6]. The source-series terminated (SST) transmitter minimizes impedance variation by increasing the passive resistor R_{SST} and reducing the voltage drop across the transistors. However, the increased size of the transistors raises the switching power at high frequencies. Therefore, a transimpedance amplifier (TIA)-based transmitter is used to reduce power consumption while controlling the output swing. In such transmitters, the impedance $(1/gm_{pn})$ variation is minimized by utilizing a complementary (CMOS) structure [10]. However, its termination impedance R_{drv} also requires

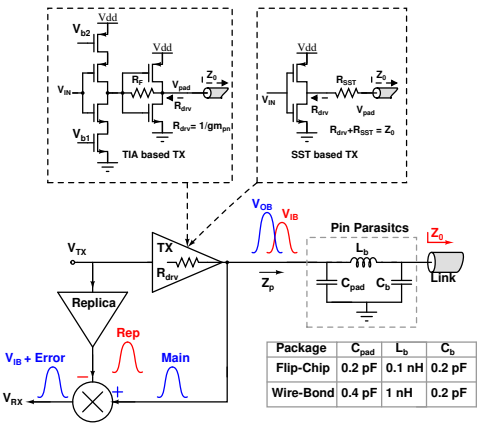


Fig. 1: Single-ended voltage-mode full-duplex transceiver.

that its current-mode pre-driver have high output impedance [11]. Furthermore, the static power in the TIA, in addition to the hybrid power, decreases energy efficiency.

In the transceivers discussed above, the channel termination is determined solely by the output impedance of the transmitter, while the impedance of the hybrid-channel interface is generally kept high. In this work, the termination is provided by a TIA-based hybrid, which generates a virtual ground for inbound signals by splitting the feedback resistor of the hybrid. Consequently, the transmitter is connected at this split node, ensuring that the output impedance of the transmitter does not affect the termination impedance. As a result, the complexity of designing the transmitter and the power consumption associated in minimizing termination variations are minimized. Moreover, the proposed architecture enables a current-mode transmitter for feedforward equalization (FFE) implementation, further reducing power consumption in compensating for channel loss.

II. Overview of SBD signaling Transceivers

A. Replica Hybrid based Voltage-Mode Transceiver

The replica hybrid-based transceiver in [7] is shown in Fig. 2(a). The V_{IN} signal is transmitted via the TIA-based transmitter. The pad node V_{pad} contains both the in-bound and out-bound signals. The hybrid uses a TIA-based current summer to sum both the replica signal $\overline{V_{IN}}$ and the signals on the pad V_{pad}. Hence, the outbound signal is gets canceled and the inbound signal can be extracted. Considering the impedance of the shunt path looking into R_{h1}, it is much higher than the termination Z_0. This condition is chosen to

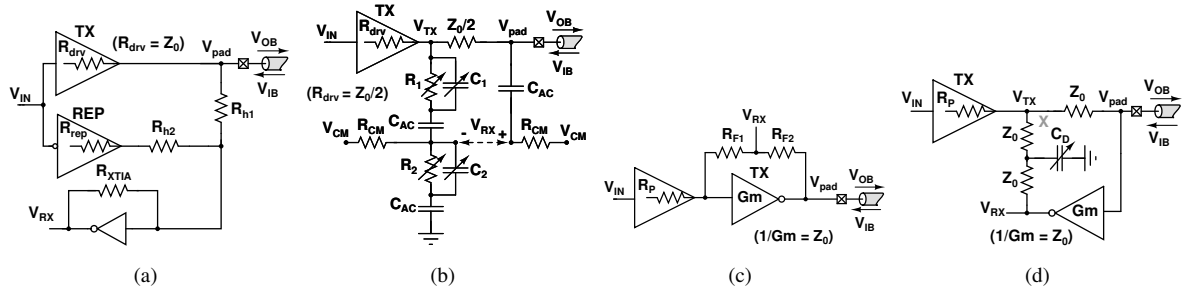


Fig. 2: (a) Replica, (b) R-Gm, (c) resistor-bridge, and (d) proposed TIA based hybrids for FD-SBD signaling.

increase the out-bound/in-bound signal swing while consuming minimal power in the hybrid.

Based on this, the total power consumption for extracting the V_{RX} signal by the hybrid can be expressed as

$$P_{Rep} = V_{DD}\left(\frac{1/Z_0^2}{2\mu C_{ox}\frac{W}{L}} + \frac{V_{RX}}{Z_0} + \frac{V_{RX}}{R_F}\right). \quad (1)$$

In this equation, the power consumption in the first term is due to the static current required for biasing the TIA transmitter. The second term accounts for the transmitter current required to extract the received signal V_{RX}, assuming the gain of the hybrid to be unity, and the third term is due to the current flowing through the resistor R_F of the TIA-transmitter for generating the outbound signal.

B. R-Gm Hybrid based Transceiver

The R-Gm hybrid-based transceiver in [6] is shown in Fig. 2(b). The hybrid splits the termination impedance into two halves and performs a weighted subtraction of the signals from the intermediate node V_{TX} and from the channel V_{pad} to eliminate the outbound signal. Thus, a separate replica driver is not required to generate the replica signal, reducing the complexity associated with the drivers. However, splitting the termination also reduces the hybrid gain to 2/3 [12]. The power consumption in this transceiver is given by

$$P_{RGm} = V_{DD}\left(\frac{2/Z_0^2}{2\mu C_{ox}\frac{W}{L}} + \frac{3V_{RX}}{2Z_0} + \frac{3V_{RX}}{2R_F}\right). \quad (2)$$

The above equation shows that the power consumption from the TIA transmitter has doubled compared to the replica hybrid. Moreover, the power consumption from remaining terms also have increased by a factor of 3/2.

C. Resistor-bridge Hybrid based Transceiver

The resistor-bridge hybrid-based transceiver as implemented in [8] is shown in Fig. 2(c). In this configuration, the TIA-based transmitter is also used as a receiver by splitting the feedback resistor R_F into R_{F1} and R_{F2} and the inbound signal is recovered between these two resistors. However, the current-mode pre-driver has finite output resistance R_P, which attenuates the inbound signal. In addition, the termination impedance also depends on R_P. The current-mode pre-driver uses a constant current source in [10], which restricts the inbound/outbound signal swing. Although the pre-driver can be replaced with VM-SST drivers, this again increases the impedance variation. In [8], a TIA-based pre-driver is used to reduce impedance variation. However, it results in increase in the static power consumption. Further, the finite R_P increases the transconductance of the TIA transmitter to match the termination, which in turn increases the power consumption. The minimum power consumption of the transceiver can be derived as

$$P_{Rb} = V_{DD}\left(\frac{1/Z_0^2}{2\mu C_{ox}\frac{W}{L}} + \frac{(R_{F1}+R_P)V_{RX}}{(R_F+R_P)Z_0} + \frac{V_{RX}}{R_P}\right). \quad (3)$$

The equation shows that the power consumption of the resistor-bridge is similar to that of the replica hybrid. However, compared to the power consumption of the replica hybrid-based transceiver including the power of replica driver and TIA-based summer, the power consumption of resistor-bridge is lesser.

III. Proposed Hybrid Transceiver

The proposed transceiver is shown in Fig. 2(d). The hybrid is designed using a TIA similar to the resistor-bridge hybrid. However, the input and output are swapped in the proposed hybrid. The input signal V_{IN} is driven through a pre-driver and a passive resistor Z_0 onto the channel. The driven input signal generates the V_{TX} signal at the transmitting node X and attenuates it to $V_{TX}/2$ in the pad, which acts as the out-bound signal V_{OB}. Simultaneously, the in-bound signal from the far-end transmitter, V_{IB}, superimposes with the out-bound signal in the pad. Based on these signals at the transmitting node and pad, we can express the relationships as

$$V_{TX} = 2V_{OB} + V_{IB}(1 - Z_0 G_m), \quad V_{pad} = V_{IB} + V_{OB}, \quad (4)$$

from which the received signal V_{RX} can be derived as

$$V_{RX} = V_{TX} - 2Z_0 G_m V_{pad}. \quad (5)$$

By tuning the transconductance G_m of the TIA equal to $1/Z_0$, the V_{RX} signal will be $-2V_{IB}$. Hence, the out-bound signal is canceled, and the in-bound signal is extracted at the V_{RX} output. As for the signal at the transmitting node V_{TX}, the in-bound signal is canceled, leaving only the out-bound signal V_{OB}. Consequently, the in-bound signal sees only the passive impedance Z_0, which matches the termination impedance. Additionally, the transmitting node does not vary with the in-bound signal. Therefore, the output impedance of the transmitter does not affect the termination impedance.

A. Hybrid Power

Based on the analysis above, the termination impedance of the proposed transceiver does not depend on the output impedance of the pre-driver. Hence, it can be designed using conventional VM drivers without the need for SST,

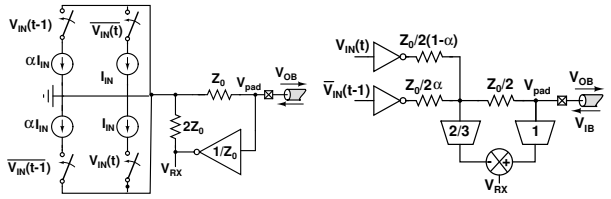


Fig. 3: FFE applied for (a) proposed transceiver, and (b) R-Gm hybrid based transceiver.

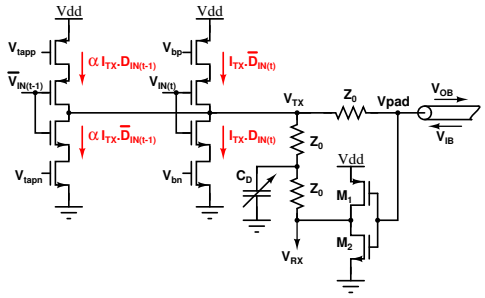


Fig. 4: Proposed transceiver with 1-tap FFE.

which reduces dynamic power and avoids static power in the TIA transmitter. The power consumption of the proposed transceiver can be derived as

$$P_{Prop} = V_{DD}\left(\frac{1/Z_0^2}{2\mu C_{ox}\frac{W}{L}} + \frac{V_{RX}}{Z_0}\right). \tag{6}$$

In the equation above, the first term represents the static power consumption in the transconductance G_m of the TIA, which is similar to the power consumption of the resistor-bridge. The second term accounts for the power consumption due to transmitter current, which is lower than that of the resistor-bridge. Additionally, the resistor-bridge consumes power due to the feedback resistor R_F, and this power consumption increases with higher data rates [6]. Therefore, the proposed transceiver consumes minimal power compared to the transceivers found in the literature.

The power consumption of the proposed transceiver is analyzed for SBD communication in long channels, which are low-pass and bandwidth-limited, necessitating high-pass equalizers to reduce ISI. The feed-forward equalizer (FFE) for the replica hybrid in [1] uses SST-based transmitters, but this increases equalization power [13]. To mitigate this, a current mode (CM) FFE is implemented in the proposed transceiver, allowing for a comparison with FFE implementations in R-GM hybrid using SST transmitters, as shown in Fig. 3. The power consumption equations for both transceivers are derived for the same received signal swing and plotted in Fig. 9(a) for two different cases, when their inputs $V_{IN}(t)$ and $V_{IN}(t-1)$ are same and when they are different. When inputs are different, the R-Gm hybrid's power consumption increases with the equalization coefficient due to the direct current path from supply to ground, raising the transmitter current. In contrast, the proposed transceiver shows lower and constant maximum power consumption with respect to the equalization coefficient.

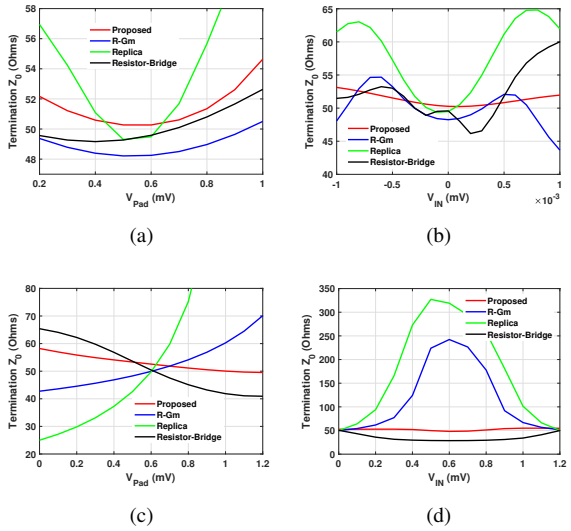


Fig. 5: Termination impedance variation for same received signal swing. With respect to variation in (a) channel voltage for TIA TX , (b) input of TIA TX, (c) channel voltage for SST TX, and (d) input of SST TX.

B. Hybrid Echo-Cancellation

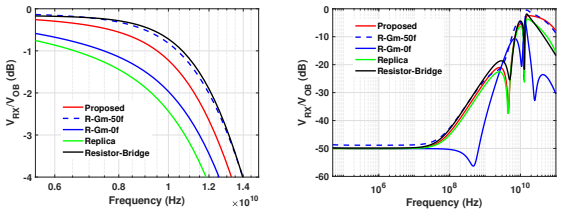
The separation of inbound and outbound signals in SBD signaling is difficult to achieve due to the mismatch between the generated replica signal and the outbound signal in the pad. The R-Gm hybrid shown in Fig. 2(b) outperforms other hybrids in echo cancellation by matching the delay between the outbound signals in the V_{TX} and V_{pad} signals. In the proposed hybrid in Fig. 2(d), the outbound signal in the V_{TX} signal and V_{pad} also experiences a similar delay given by the time constant $Z_0.C_{pad}/2$. Hence, the feedback resistor $2Z_0$ is split into two halves and by using a capacitor C_D a delay for the outbound signal is introduced to match the delay of V_{RX} signal. Therefore, by matching capacitor $C_D$with the pad capacitor, the echo is minimized. However, the near-end reflection due to package parasitics requires background echo cancellation using FIR filters [5], [9].

C. Circuit Implementation

The circuit implementation of the proposed transceiver is shown in Fig. 4. The transconductance (Gm) of the TIA is designed using a CMOS structure formed by the transistors (M_1, M_2). For a 50 Ω characteristic impedance in the channel, the W/L ratio of each transistor is fixed to achieve a Gm of 10 mS. However, the finite output impedance due to channel-length modulation increases the Gm. Additionally, PVT variations must also be compensated. Thus, the Gm can be split into multiple cells connected in parallel based on a thermometer-coded binary DAC to minimize these variations. The capacitor C_D can also be implemented using a binary-weighted capacitive DAC based on the pad capacitance C_{pad}. The filter coefficients for main and post cursors are designed using a CMOS structure with source and sink current sources driving currents I_{TX} and αI_{TX}. The tap coefficient can be easily tuned without affecting the termination impedance.

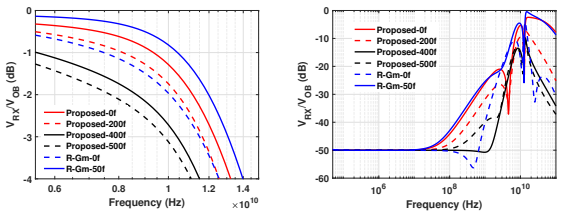
IV. Simulation Results

The proposed transceiver is designed using the TSMC PDK in 65 nm technology and simulated using the Spectre in



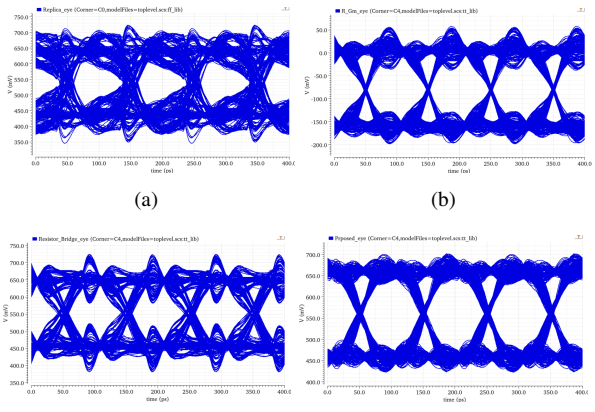
(a) (b)

Fig. 6: Frequency characteristics of the hybrids: (a) bandwidth and (b) echo-cancellation.



(a) (b)

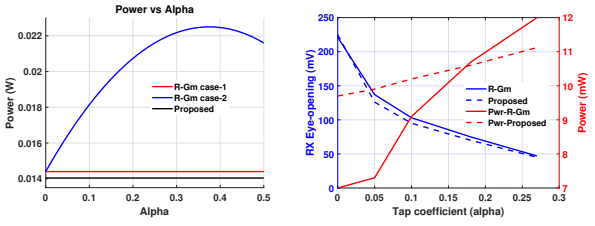
Fig. 7: Frequency characteristics of the proposed hybrid for variation in C_D: (a) bandwidth and (b) echo-cancellation.



(a) (b)

(c) (d)

Fig. 8: Full-duplex eye-diagrams of hybrids (a) replica, (b) R-Gm, (c) resistor-bridge, and (d) proposed.



(a) (b)

Fig. 9: Data-dependent power consumption with respect to tap coefficient α in the following transceivers with (a) proposed hybrid, and (d) R-Gm hybrid.

Cadence Virtuoso. The variation of the termination impedance of the proposed transceiver is compared with that of the transceivers in Fig. 2, for the same received signal swing. The impedance variation, plotted with respect to V_{Pad} and V_{IN} voltages while using TIA and SST-based transmitters are shown in Fig. 5. The impedance variation with the TIA-based transmitter is similar for all transceivers. However, when using the SST-based transmitter, the impedance variation is minimized in the proposed transceiver.

The received signal bandwidth of the proposed hybrid is compared with other hybrids in Fig. 6(a), by considering the package parasitics in Fig. 1. The plot indicates that the resistor-bridge hybrid has a higher bandwidth than the proposed hybrid.

TABLE I: Comparison with conventional transceivers.

Ref	Tech. (nm)	Data-rate (Gb/s)	Supply (V)	Channel Loss @ Nyq.(dB)	Power (mW)	FOM (pJ/b)
This Work	**65**	**20**^{a} **TX-CM/TIA based Proposed Hybrid**	**1.2**	**<1 dB**	**7**^{a}	**0.35**^{a}
[7]	5	50.4^c (FD:25.2+25.2) TX-SST/Replica Hybrid	0.75	1.2 mm Interposer 4.5 dB	3.375^c	0.067^c
[8]	65	15^c (FD:7.5+7.5) TX-TIA/Resistor-Bridge Hybrid	1.2	10 mm FR4 2.5 dB	10.1^c	0.67^c
[6]	16	32^b (FD:16+16) TX-TIA/R-Gm Hybrid	0.9	5 mm < 1 dB	13.44^b	0.42^b

^{a} Simulated. ^{b} Post-layout Simulated. ^{c} Measured.

The R-Gm and replica hybrids exhibit a high time constant in the interface between the subtractor and channel, which decreases their bandwidth. The bandwidth of the resistor-bridge hybrid is higher due to the zero created by the feedback resistor R_F and the capacitance at the input of the TIA. However, this also causes high-frequency termination variation and induces reflections. In case of the echo cancellation bandwidth shown in Fig. 6(b), the R-Gm hybrid outperforms all the hybrids. However, the echo cancellation bandwidth in Fig. 7(b), is improved in the proposed hybrid by matching capacitor C_D with the pad capacitance. The variation in C_D also introduces a trade-off between bandwidth and echo cancellation, as illustrated in Fig. 6(a). A similar trade-off is found in the R-Gm hybrid when creating a zero in the subtractor interface with capacitor C_1. Thus, the optimum value of C_D is chosen based on the SBD eye diagram.

The test bench involves all the transceivers shown in Fig. 2, simulated at a 20 Gb/s SBD data rate, including package parasitics. While signaling in a short channel, the eye diagram of the proposed transceiver, after tuning capacitor C_D, is similar to that of the R-Gm hybrid, as shown in Fig. **??**. The eye opening of the proposed transceiver compared to the R-Gm hybrid for different channel losses as shown in Fig. 9(b). The eye opening after tuning the FFE tap coefficient is similar for both transceivers. However, the power consumption of the R-Gm hybrid during signaling in high-loss channels increase more than that of the proposed transceiver. Table 1 compares the proposed architecture with recent literature.

V. Conclusion

This paper presents a single-ended voltage-mode simultaneous bidirectional (SBD) transceiver for chip-to-chip interconnects. A hybrid network in the receive path cancels the transmitted signal to extract the received signal, enabling efficient bidirectional communication. Unlike conventional source-series terminated (SST) and trans-impedance amplifier (TIA)-based transmitters, which consume high power to minimize output impedance variation, the proposed design mitigates this variation, allowing for a low-power transmitter. In addition the power consumption in incorporating voltage mode feed-forward equalizer (FFE) is reduced by using current mode taps in the proposed transceiver. Implemented using TSMC PDK in 65 nm technology and the simulation results gives an energy efficiency of 0.35 pJ/b at 20 Gb/s SBD data-rate.

VI. Acknowledgement

We acknowledge the support of Synopsys, Inc., Sunnyvale, USA, for this work.

REFERENCES

[1] S. Mukherjee, A. Das, S. Seth, and S. Saxena, "An energy-efficient 3gb/s pam4 full-duplex transmitter with 2-tap feed forward equalizer," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 5, pp. 916–920, 2020.

[2] R. Farjadrad, K. Kaviani, D. Nguyen, M. Brown, G. Geelen, C. Bastiaansen, N. Rao, V. Popuri, G. Shen, H. Khatibi *et al.*, "11.8 an echo-cancelling front-end for 112gb/s pam-4 simultaneous bidirectional signaling in 14nm cmos," in *2021 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 64. IEEE, 2021, pp. 194–196.

[3] B. Casper, A. Martin, J. E. Jaussi, J. Kennedy, and R. Mooney, "An 8-gb/s simultaneous bidirectional link with on-die waveform capture," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 12, pp. 2111–2120, 2003.

[4] H. Tamura, M. Kibune, Y. Takahashi, Y. Doi, T. Chiba, H. Higashi, H. Takauchi, H. Ishida, and K. Gotoh, "5 gb/s bidirectional balanced-line link compliant with plesiochronous clocking," in *2001 IEEE International Solid-State Circuits Conference. Digest of Technical Papers. ISSCC (Cat. No. 01CH37177)*. IEEE, 2001, pp. 64–65.

[5] S. Goyal, G. Parulekar, and S. Gupta, "A true full-duplex io (tfd-io) with background si cancellation for high-density interfaces," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 30, no. 5, pp. 615–624, 2022.

[6] D. Jarrett-Amor, K. Yadav, D. Zhang, B. Yang, S. Jalali, and T. C. Carusone, "A 32 gb/s, 0.42 pj/bit passive hybrid simultaneous bidirectional transceiver for die-to-die links," in *2023 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2023, pp. 1–5.

[7] Y. Nishi, J. W. Poulton, W. J. Turner, X. Chen, S. Song, B. Zimmer, S. G. Tell, N. Nedovic, J. M. Wilson, W. J. Dally, and C. T. Gray, "A 0.297-pj/bit 50.4-gb/s/wire inverter-based short-reach simultaneous bi-directional transceiver for die-to-die interface in 5-nm cmos," *IEEE Journal of Solid-State Circuits*, vol. 58, no. 4, pp. 1062–1073, 2023.

[8] C. Yuan, A. Naguib, and S. Shekhar, "On the design of low-power hybrids for full duplex simultaneous bidirectional signaling links," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 4, pp. 1413–1422, 2020.

[9] Y.-H. Fan, A. Kumar, T. Iwai, A. Roshan-Zamir, S. Cai, B. Sun, and S. Palermo, "A 32-gb/s simultaneous bidirectional source-synchronous transceiver with adaptive echo cancellation techniques," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 2, pp. 439–451, 2019.

[10] W. Bae, "Cmos inverter as analog circuit: An overview," *Journal of Low Power Electronics and Applications*, vol. 9, no. 3, p. 26, 2019.

[11] D. Jarrett-Amor and T. C. Carusone, "A 16 gbps, 0.126 pj/bit, single-ended tia driver with impedance peaking control for sbd d2d links," in *2024 22nd IEEE Interregional NEWCAS Conference (NEWCAS)*. IEEE, 2024, pp. 45–49.

[12] V. K. Surya, S. K. Prusty, B. D. Sahoo, and N. Wary, "Energy efficient resistor-transconductor hybrid-based full-duplex transceiver for serial link," *IEEE Transactions on Circuits and Systems I: Regular Papers*, pp. 1–0, 2024.

[13] C. Fan, W.-H. Yu, P.-I. Mak, and R. P. Martins, "A 40-gb/s pam-4 transmitter using a 0.16-pj/bit sst-cml-hybrid (sch) output driver and a hybrid-path 3-tap ffe scheme in 28-nm cmos," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 12, pp. 4850–4861, 2019.