A BW-Extended Multi-Band Receiver with High-Order N-Path Filtering at RF Front-End and BB Achieving 200MHz BW and 36.5dBm OB-IIP$_3$

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2025 IEEE International Symposium on Circuits and Systems (ISCAS) | 979-8-3503-5683-0/25/$31.00 ©2025 IEEE | DOI: 10.1109/ISCAS56072.2025.11043245

***Abstract*—This work presents a radio-frequency (RF) blocker-tolerant multi-band (0.5 to 2GHz) receiver to achieve both wide passband bandwidth (BW) and sharp out-of-band (OB) attenuation at near-by frequency. At RF front-end, it features the combination of the 4th-order N-path low-noise transconductance amplifier (LNTA) and the bottom-plate N-path filter, while at baseband (BB) it introduces the 3rd-order N-path lowpass filter and 2nd-order BB trans-impedance amplifier (TIA). Besides, a negative-feedback frequency-translational loop is created to achieve the input-impedance matching condition. Designed in 65nm CMOS technology, our receiver achieves -220dB/decade near-by roll-off slope for a 200MHz RF-BW at 2GHz. With 3xRF-BW offset, the receiver achieves 36.5dBm OB-IIP3. The noise figure (NF) is simulated from 2.4 to 3.8dB and the power consumption is 27.6 to 37.8mW. The chip area is 0.68mm^2.**

Keywords—Linearity, low-noise transconductance amplifier, LO generator, N-path filter, notch, noise figure, OOB-IIP$_3$, receiver, roll-off slope.

I. Introduction

With the continuous development on wireless communications, it brings several challenges in the design of sub-6GHz radio-frequency (RF) receivers, especially for the frequency-division duplexing (FDD) operation in the 5G-New Radio (NR) communication. Firstly, the passband BW increases to >100MHz in order to guarantee the high-speed wireless data transmission, while the frequency separation (Δf) between the transmitter and receiver reduces to less than twice the RF-bandwidth (BW). Therefore, the receivers must provide sufficient sharp out-of-band (OB) rejection on transmitter leakage signal and meanwhile with wide passband BW. Secondly, the linearity of the receivers must be high to make sure the quality of the in-band signal, since there maybe exist signals due to the carrier aggregation or the digital beamforming operation. Traditionally, the mixer-first receiver [1, 2] can be considered as a promising candidate due to its high OB linearity (i.e., 27dBm OB-IIP$_3$), since it delays the signal amplification to baseband (BB) and provides OB rejection by translating a lowpass filtering at BB to a bandpass response at RF. However, the NF (5.5dB) and power consumption (60mW) are sacrificed. In order to break such tradeoff between the linearity and NF, in [3] an auxiliary noise-cancelling path is introduced to cancel the thermal of antenna (50Ω in typical) and transconductance amplifier at input. Thus, it simultaneously achieves 13.5dBm OOB-IIP$_3$ and only 1.9dB NF. However, it also comes at the cost of chip area (1.2mm^2) and power consumption (78mW). In addition, [4] enhance OB attenuation by introducing complex poles to achieve -40dB/decade roll-off slope, but the passband BW is only 20MHz and also with high power consumption (179mW). In this work, we report a multi-band RF receiver by featuring both wide passband BW and sharp near-by roll-off slope. It employs a high-order N-path RF front-end (a 4th-order N-path LNTA and a bottom-plate N-path filter) to provide high-Q bandpass filtering response, BB 3rd-order N-path lowpass filter and 2nd-order TIA to further enhance the OB rejection. Besides, the input-impedance matching condition is achieved by the negative-feedback loop around the receiver. Designed in 65nm CMOS technology, our receivers presents both high linearity (36.5dBm OB-IIP$_3$), wide passband BW (200MHz RF-BW) and low NF (2.4 to 3.8dB), while only consuming 27.6 to 37.8mW power consumption for 0.5 to 2GHz RF range and occupying 0.68mm^2 chip area.

II. Implementation Details

Fig. 1 shows the block diagram of our proposed receiver, which consists with a high-order N-path RF front-end, passive mixer, BB N-path lowpass filter and 2nd-order BB trans-impedance amplifier (TIA), also with a negative-feedback frequency-translational loop for input-impedance matching. The bottom-plate N-path filter is introduced at the RF input to enhance the linearity and avoid the saturation of 4th-order N-path low-noise transconductance amplifier (LNTA). The LNTA [Fig. 2(a)] provides voltage gain at in-band to decrease the noise contribution of the following stages, and achieves sharp rejection for blockers at near-by frequency. When the RF signal is amplified by LNTA, it will be down-converted by mixers (i.e., passive switches) and looks the BB 3rd-order N-path lowpass filter, which creates near-by notch response to further enhance the OB rejection. Finally, the signal is amplified by a BB 2nd-order trans-impedance amplifier (TIA), which achieves wide passband BW by creating complex poles. Both the 4th-order N-path LNTA and mixers are driven by 25%-duty-cycle non-overlapping LO waveforms (i.e., RF-LO$_1$ to RF-LO$_4$), while the BB 3rd-order N-path lowpass filter is driven by 25%-duty-cycle non-overlapping LO waveforms at BB frequency (i.e., BB-LO$_1$ to BB-LO$_4$). In addition, in order to provide an extra freedom on the design of LNTA, a negative-feedback frequency-translational loop is created around the receiver to provide the input-impedance matching condition.

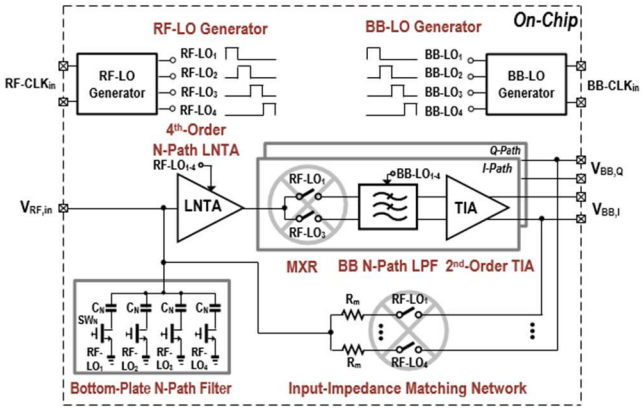

Fig. 1. The block diagram of the proposed multi-band RF receiver.

A. High-Order N-Path RF Front-End

The RF front-end is consisted with a 4th-order N-path LNTA and a 2nd-order bottom-plate N-path filter, which enables for both wideband passband BW and sharp OB roll-oof slope. Fig. 2(a) shows the 4th-order N-path LNTA [5], in which the RF signal is amplified by $-G_{m,RF}$. The near-by blocker rejection network is connected around $-G_{m,RF}$, which can be modeled as a 4th-order LC network (connecting a series N-path network and a paralleled N-path network in series). Here, the series N-path network is created by introducing a gyrator (G_{ma} and G_{mb}). In Fig. 2(b), two zeros are created at nearby sideband around the center frequency. To attenuate the OB blockers, an extra N-path network (i.e., OB blocker rejection network) is introduced. In simulations, the OB rejection improves 19.5dB thanks to the OB blocker rejection network. Note that we can adjust the product of G_{ma} and G_{mb} to modify the zero frequency. Here, G_{ma} and G_{mb} are 8.1 and 21.2mS, respectively. Besides, in order to prevent the blocker signal coming into the receiver, a bottom-plate N-path filter [6] is introduced at the RF input (Fig. 1), which can effectively avoid gain compression of the LNTA. When compared to the traditional top-plate N-path filter in which the capacitor is connected to the ground side, the bottom-plate N-path filter manifests 5.5 and 8.2dB IIP_3 improvement for the OB and in-band operation, respectively.

B. Baseband 3rd-Order N-path Lowpass Filter

In order to further enhance the OB attenuation, a BB 3rd-order N-path lowpass filter [7] is employed after the mixer, as shown in Fig. 3. The 3rd-order N-path lowpass filter is based on an N-path notch network (BB switches and series capacitor C_2) to create zero and suppress the OB blockers, which can be modeled by a series RLC resonator. The notch position is defined by BB-LO frequency. Capacitor C_1 is employed at both the input and output of the filter, which enables attenuation at far-out frequency. Interestingly, the shunt capacitor C_3 added between the switches can be taken as a negative resistor, since it changes the phase shift between the output current and V_{in} (e.g., <90°). Thus, C_3 can be optimized to cancel part of the paralleled resistor R_P in the RLC resonator and increase the Q factor. When choosing C_1=10pF, C_2=6.3pF, C_3=3.2pF and the BB switches with 80μm/60μm, the simulated S_{21} of the 3rd-order BB N-path lowpass filter

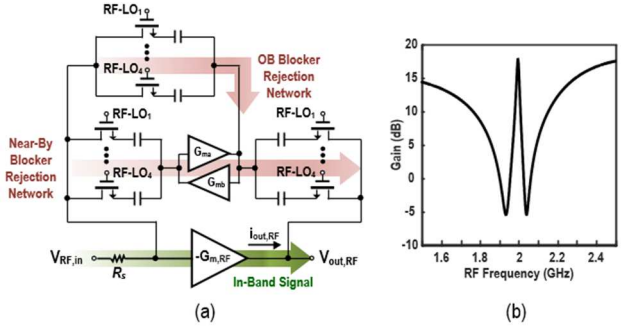

Fig. 2. (a) Schematic of the 4th-order N-path LNA. (b) Simulated gain response with the OB blocker rejection network.

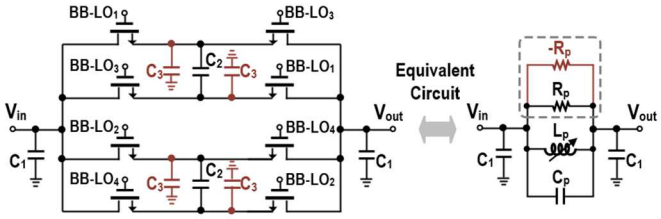

Fig. 3. Schematic of the BB N-path lowpass filter and its equivalent circuit.

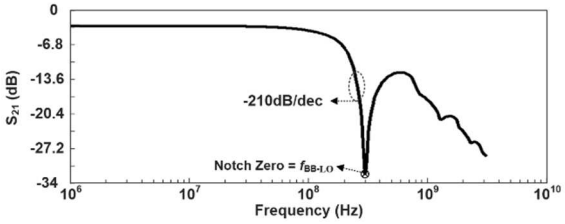

Fig. 4. Simulated S_{21} of the BB N-path lowpass filter.

shows -210dB/decade roll-off slope at near-by OB frequency in Fig. 4, when the BB-LO frequency is defined by 300MHz.

C. Baseband 2nd-Order TIA

A 2nd-order TIA with conjugate complex poles is employed to achieve an OB filtering slope of -40dB/decade, thereby enhancing the OB linearity and resolving the interference issue of OB blocker signals. In Fig. 5(a), the circuitry of the 2nd-order TIA is shown, in which $-G_{m,BB}$ amplifies the BB signal and the current-to-voltage gain is achieved by the feedback resistor R_F. The input capacitor C_{in} helps on improving the linearity by shunting the blockers' current, while the load capacitor C_L helps on creating 2nd-order response. R_F is designed in tunable to adjusting the TIA gain. According to the equivalent circuit model in Fig. 5(b), the transfer function is

$$\frac{V_{out}}{I_{in}}(s) \approx \frac{-R_F}{\frac{R_F C_{in} C_L}{g_{m,BB}} s^2 + \left(\frac{R_F + r_o}{g_{m,BB} R_o} C_{in} + \frac{C_L}{g_{m,BB}}\right) s + 1} \qquad (1)$$

, in which $g_{m,BB}$ and r_o are the transconductance and output resistance of $-G_{m,BB}$, respectively. In this design, C_{in}=10pF, C_L=5pF, R_F=2kΩ and $g_{m,BB}$=56mS are chosen to achieve 100MHz BB-BW and -40dB/decade OB roll-off slope. In Fig. 6, the OB rejection at 300MHz offset of our 2nd-order TIA is 6.7dB larger than the 1st-order one. Note that sufficient phase margin (i.e., >65°) is provided to guarantee the TIA is stable.

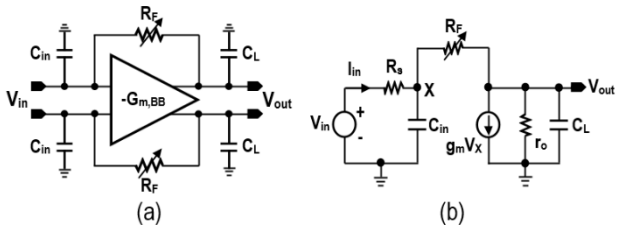

Fig. 5. Circuitry of (a) the 2nd-order BB TIA and (b) its equivalent circuit model.

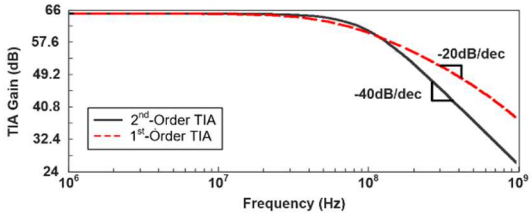

Fig. 6. The 2nd-order BB TIA shows wider passband BW and sharper OB roll-off slope when compared to the 1st-order one.

D. Frequency-Translational Loop

In order to achieve an input-impedance matching for 0.5 to 2GHz, we use a negative-feedback frequency-translational loop (Fig. 1). The frequency-translational loop upconverts the BB TIA output voltage signals into a RF voltage signal, and meanwhile returns the RF voltage signal to the RF input in the form of the voltage-current negative feedback through the matching resistor R_{match}. From the impedance view, the frequency-translational loop upconverts the BB lowpass impedance to RF bandpass impedance at the receiver input. Thus, the input impedance Z_{in} of the receiver is:

$$Z_{in} = \frac{R_{\text{match}} // Z_{LNTA} // Z_{NP}}{1 + A_0} \quad (2)$$

, where Z_{LNTA} and Z_{NP} are the input impedance of the LNTA and N-path filter, respectively, and A_0 is the loop gain of the frequency-translational loop, that is,

$$A_0 = A_{LNTA} \times A_{Mixer}^2 \times A_{LPF} \times A_{TIA} \quad (3)$$

. Therefore, the input-impedance matching condition can be achieved by adjusting R_{match}. In this design, the A_0 is ~0.12dB and R_{match} is 2.1kΩ. Note the function of N-path filter mainly provides extra OB rejection and its in-band impedance Z_{NP} is much larger when compared to Z_{LNTA}.

E. Low-Noise 25%-Duty-Cycle Non-overlap LO Generator

The block diagram of the 25%-duty-cycle non-overlapping LO generator for both RF switches and BB switches are shown in Fig. 7. Master clocks, $CLK_{IN,P}$ and $CLK_{IN,N}$, are injected and amplified by an input buffer. After adjusted by a phase corrector, the clocks $2LO_{P,N}$ are injected to "divider-by-2". When applying "AND" logic, we get the 25%-duty-cycle LO waveforms. They will be amplified by output buffer and drive the RF and BB switches by RF-LO_{1-4} and BB-LO_{1-4}, respectively. In this design, the phase noise of the 25%-duty-cycle LO waveforms are mainly due to the input buffer and the noise of the module "divider-by-2" almost does not appear to the output, since both the rising and falling edges of RF-LO_{1-4} and BB-LO_{1-4} are from $2LO_P$ and $2LO_N$. In simulation, the low-noise LO generator shows -167 and -164.4dBc/Hz phase noise at 80MHz offset at 0.5 and 2GHz, respectively. The simulated power consumption is 13.6mW/GHz.

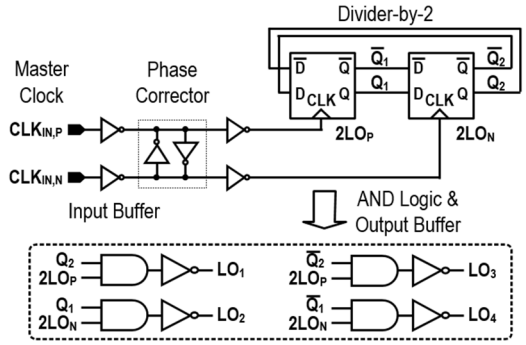

Fig. 7. Block diagram of the 25%-duty-cycle non-overlap LO generators for both RF and BB.

III. Simulation Results

The layout of our proposed multi-band receiver is shown in Fig. 8, which is designed in 65nm CMOS process. The chip area is 0.68mm^2. The power supply is 1.2V and the power consumption increases from 27.6 to 37.8mW when covering 0.5 to 2GHz. The power consumption of -$G_{m,RF}$ and -$G_{m,BB}$ are 4.5 and 6.1mW, respectively. In this design, both the bonding wires' inductive effect and the PADs' parasitic capacitance are included in simulations. The simulated receiver gain response is shown in Fig. 9 when f_{LO} is 2GHz, in which the passband gain is 28dB and the BB-BW is 100MHz. The near-by roll-off slope reaches -220dB/decade thanks to the BB N-path filter. The notch frequency falls in 300MHz, which is defined by BB-LO. At 2xRF-BW (i.e., 400MHz) offset, the OB rejection can still guarantee 33dB to attenuate blockers. When covering 0.5 to 2GHz, the simulated conversion gain drops from 31 to 28dB due to the parasitic capacitance. In Fig. 10, the simulated input-impedance matching (S_{11}) is shown, which is <-10dB for the frequency range of 0.5 to 2GHz, defined by RF-LO.

Fig. 11 presents the simulated IIP_2 and IIP_3 performance for both in-band and OB operation at 2GHz. When operating at in-band (e.g., Δf/RF-BW=0.1), the IIP_2 and IIP_3 are 33.6 and -7.8dBm, respectively. When the offset frequency increases to 1xRF-BW, the IIP3 becomes 22.3dBm. When operating at OB (e.g., Δf/RF-BW=3), the IIP_2 and IIP_3 are 57.7 and 36.5dBm, respectively. Besides, the blocker-caused in-band -1-dB gain compression (B_{-1dB}) is simulated 0dBm when the blocker signal is injected to the receiver input at 2xRF-BW offset for f_{LO}=2GHz. Note that the linearity is mainly limited by -$G_{m,RF}$ and -$G_{m,BB}$, which are the only two active parts in the signal path. Fig. 12 shows the simulated NF performance, which covers from 2.4 to 3.8dB for 0.5 to 2GHz. The NF can be improved by increasing the voltage gain of LNA but at the cost of the linearity. Besides, when injecting a blocker signal at the receiver input at 2.5xRF-BW offset when f_{LO}=2GHz, the NF goes up to 5.6dB for -10dBm blocker power. The simulated LO leakage at receiver input is -53dBm at 2GHz and the power consumption is simulated 27.6 to 37.8mW for 0.5 to 2GHz. The performance of our proposed receiver is summarized and compared to the state-of-the-art as shown in Table I. It mainly features wide passband BW, high linearity (i.e., OB-IIP_3) and

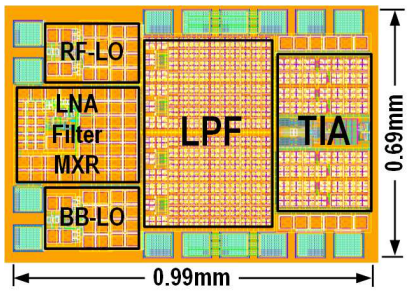

Fig. 8. Layout of our proposed multi-band RF receiver in 65nm CMOS process.

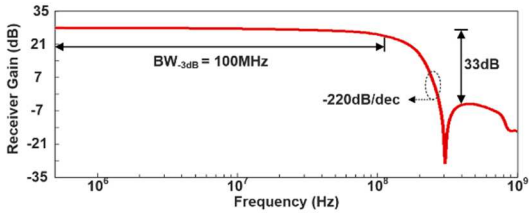

Fig. 9. Simulated receiver gain response at 2 GHz, presenting -220 dB/dec roll-off slope at near-by frequency and 100 MHz BB BW_{-3dB}.

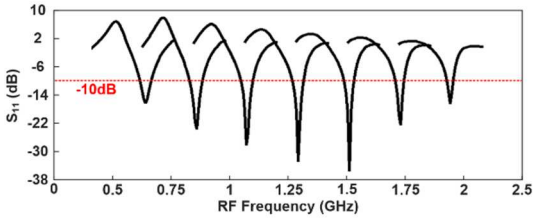

Fig. 10. Simulated receiver S_{11} (input-impedance matching) for different RF frequency.

low NF, meanwhile with comparable power consumption, active area and conversion gain.

IV. Conclusions

In this work, we propose a blocker-tolerant multi-band receiver by employing a 4th-order N-path LNTA and a N-path filter with bottom-plate technique to provide high-Q bandpass filtering response at RF, and a BB 3rd-order N-path lowpass filter to further enhance the OB rejection. Designed in 65nm CMOS, our receivers presents both high linearity (36.5dBm OB-IIP_3), wide passband BW (200MHz RF-BW) and low NF (2.4 to 3.8dB), while only consuming 27.6 to 37.8mW power consumption for 0.5 to 2GHz RF range and occupying 0.68mm^2 chip area.

Acknowledgment

This work was supported in part by the National Natural Science Foundation of China (NSFC) under Grant 62104263, in part by GuangDong Basic and Applied Basic Research Foundation under Grant 2022A1515-012295 and in part by the Guangdong Zhujiang Project under Grant 2021ZT09X070.

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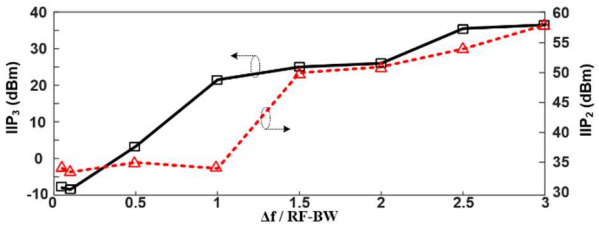

Fig. 11. Simulated IIP_3 and IIP_2 profiles for different Δf/RF-BW ratio.

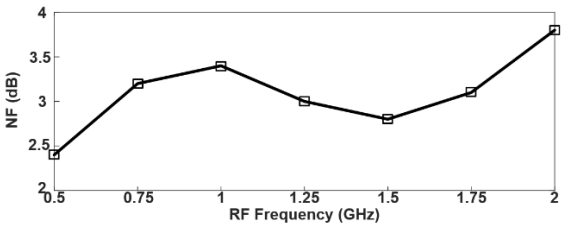

Fig. 12. Simulated NF for different RF frequency.

TABLE I. Comparision with State-of-the-Art

	This Work #	ISSCC'21 [5]	JSSC'20 [4]	JSSC'19 [6]	JSSC'18 [8]
Topology	**BW-Extended RX w/ both RF and BB N-path Filters**	LNTA-Based RX w/ 2nd-Order TIA and Zero	Mixer-First RX w/ BW-Extended BB-TIA	N-path RX w/ Bottom-Plate Mixing	Gain-Boosted N-path LNA w/ Shunt LC
RF Input Style	Single-Ended	Single-Ended	Single-Ended	Differential	Single-Ended
RF Range (GHz)	0.5 to 2	0.4 to 3.2	0.2 to 2	0.1 to 2	0.7 to 1
RF BW (MHz)	**200**	160	18	13	8*
Voltage Gain (dB)	28 to 31	36	13	16	4.8 to 5.5
DSB NF (dB)	**2.4 to 3.8**	2.7 to 3.6	4.3 to 7.6	4.1 to 10.3	8.7 to 9.2&
B_{-1dB} (dBm) @ Offset (MHz)	**0 @ 2xBW**	-5* @ 5xBW	6* @ 4.5xBW	6 @ 2.3xBW	8
OB-IIP_3 (dBm)	**36.5 (Δf=3xBW)**	13 (Δf=5xBW)	24* (Δf=4.5xBW)	44 (Δf=6xBW)	32.3 (Δf=5xBW)
Power (mW)	**27.6 to 37.8**	65.5 to 114.8	147 to 179	34 to 96	62.5
Supply (V)	1.2	1.3/1.2	1.2	1,2, 1	1.5
Die Size (mm^2)	0.68	0.6	0.48	1	2.2
Technology	65nm CMOS	40nm CMOS	28nm CMOS	28nm CMOS	180nm SOI

* Estimate from figure, # Based on simulation results.

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