A 50 Gb/s Rad-Hard Quad TIA IC for Onboard Satellite Interconnects

Philip Ostrovskyy
IHP - Leibniz-Institut für innovative Mikroelektronik
Frankfurt (Oder), Germany

Aintzane Lujambio
ALTER TECHNOLOGY
Sevilla, Spain

David Lobato
ALTER TECHNOLOGY
Sevilla, Spain

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***Abstract*—Energy efficiency is one of the most important factors while designing integrated circuits for space applications. At the same time, an IC must operate correctly despite of harsh space environment. This paper demonstrates a quad channel transimpedance amplifier (TIA) integrated circuit that aims to simultaneously achieve high data rates, radiation hardening, and high energy efficiency. To optimize TIA operation with respect to bandwidth, gain, power consumption, we implemented a digital controlling interface driving low speed DACs for adjusting currents in different TIA stages. The complete circuit has been manufactured in a 130 nm SiGe BiCMOS semiconductor process. Electrical probe testing shows the achievable data rate of more than 50 Gb/s in each channel. The implemented on-chip low dropout regulators provide an operation from a single supply voltage. The TIA IC was exposed to proton and gamma radiation. At a 2.5 V supply voltage the minimum power efficiency of 1.35 pJ/bit is demonstrated.**

***Index Terms*—transimpedance amplifier, optical receiver, radiation hardening, space application.**

I. Introduction

The rise of high-definition streaming, cloud-based services, and remote work drives the development of wireless and wireline communication systems towards higher bandwidth, data rates, channel spectral efficiencies since last decades. This race for data speed has a direct impact on satellite communication systems as well, demanding higher transmission data rates in space. Having the same technical goal with respect to receive, transmit and route of the communication signals, satellite communication systems have more demanding requirements due to launch to the orbit and harsh operation environment that limits the straightforward use of existing ground-based communication system principles. The focus on optimizing the size, weight and power of satellite payloads has led to the use of a digital transparent processor (DTP) approach [1]. This allows the routing of signals without the need for demodulation and decoding, while also providing a high level of channel configurability and power efficiency. This technique has been developed even further by using a light weight optical switch to commutate the signals within a satellite [2]. Fig. 1 shows a block diagram of the multi-antenna satellite payload utilizing the optical fiber switch to route the signals between different wireless transceivers (TRx).

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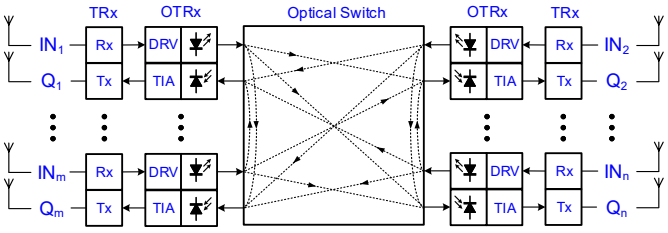

Fig. 1: Simplified block diagram of a MIMO transceiver payload utilizing optical-to-electrical and electrical-to-optical conversions to perform routing of the downconverted signals.

The received radio signal is downconverted to the intermediate frequency, where it is digitized by an ADC. After being serialized, a bit stream comes to the driver (DRV) that drives a laser diode. Here, the signal is converted to the optical domain and routed to the dedicated path by the optical switch. At the output of the optical switch, the optical receiver consisting of a photodetector and TIA performs a conversion into the electrical domain. Then, the recovered electrical signal goes through the reverse conversion steps in the radio transmitter: deserialization, digital-to-analog conversion, upconversion to the carrier frequency. As the weight of the MIMO transceiver payload can be substantially reduced by using optical interconnects, the power consumption of an optical transceiver module and especially its electrical parts still have to be optimized. The TIA IC following a photodetector builds an optical receiver, which together with optical transmitter including a laser diode and a driver completes the optical transceiver module. The TIA IC reported in this paper is intended to be a part of a quad-channel optical transceiver module [3]. It will be flip-chip mounted in the module, together with another ICs, photodiode and laser diode arrays. This paper presents the radiation hardening design approach, electrical experimental results and irradiation testing of the quad-channel TIA IC.

II. TIA Circuit Design

Each TIA channel includes a TIA core, two stage intermediate gain amplifier and a 100 Ohm differential output buffer. Fig. 2 shows a schematic of one TIA channel. A TIA core consists of a common-emitter amplifier Q_1, emitter-follower Q_2 and a resistive shunt feedback R_F. This architecture demon-

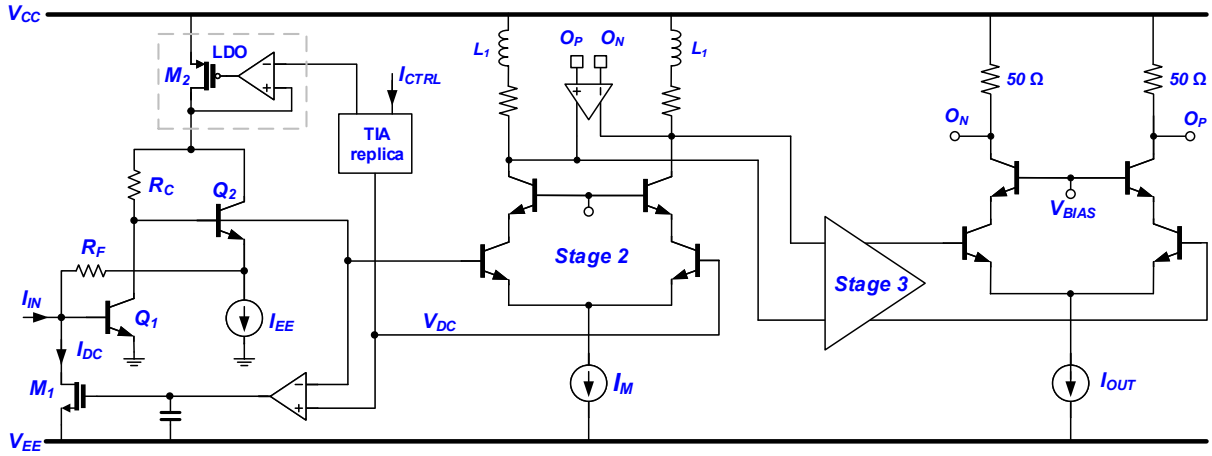

Fig. 2: Schematic of the TIA channel.

strates broadband operation and good noise performance [4]. In the quad channel TIA configuration, to improve isolation between the channels, a low-dropout regulator (LDO) for each TIA core circuit has been used. A TIA replica represents the same structure as a TIA core, however scaled down to be biased at five times less current. It provides a reference voltage for the LDO. A TIA replica bias current I_{CTRL} can be digitally controlled in a way that the LDO output voltage can be set in a range from 2 V to 2.4 V.

Additionally, an overcurrent protection circuit consisting of an opamp driving transistor *M1* protects the input TIA from the overload current coming from photodetector in case e.g. of a back-to-back test in the optical transceiver module. Gain stages 2 and 3 in Fig. 2 represent two identical differential cascode amplifiers with inductive peaking load. The stage 2 receives the HF signal from the TIA core while a DC output from the TIA replica is applied to the complementary input. In both stages, inductors *L1* and *L2* with a 370 pH value have been used for bandwidth extension. Because of the single-ended TIA input and high gain in the following differential stages, the DC offset can occur at the TIA outputs. In order to correct it, a DC-offset compensation feedback senses the DC difference at the output of the TIA channel and corrects it by regulating DC levels at the output node of the first intermediate gain stage. The output buffer is realized as a cascode differential pair with a load resistance of 50 Ohm at each branch. This value minimizes the TIA output reflection losses in presence of the on-board transmission line.

III. Radiation Hardening Design Approach

A fast, robust and programmable TIA circuit requires broadband high-speed amplification stages, operational amplifiers in compensation loops and digital control circuits. For this purpose a SiGe BiCMOS technology is a good candidate providing HBT transistors for high speed operation and CMOS components to realize OAs and digital logic. Because of the mixed-signal nature of the TIA circuit which utilize CMOS and SiGe HBTs, various design considerations have been applied to make this IC tolerable to different radiation effects. The major radiation effects degrading the IC performance are total ionizing dose (TID) and single event effects (SEE).

A high frequency path of the TIA was designed using SiGe HBT transistors in order to achieve high data rate. At the same time, SiGe HBT transistors are known to withstand high ionizing doses because of their high radiation tolerance with respect to gamma rays, neutrons and protons [6]. In the chosen technology, a SiGe HBT NPN transistor can tolerate up to a 1.2 MRad TID value [5]. On the other hand, all operational amplifiers, OTAs, SPI and digital IO cells use CMOS devices, which are more prone to ionizing radiation effects. This may result in increased leakage currents and threshold voltage deviations. In this design, the high-voltage (HV) NMOS devices operating at 3.3 V supply have been replaced by the enclosed-layout transistors in order to boost the TID value up to 1 Mrad [7]. This is especially critical for a wide HV NMOS in the digital IO cells, where transistors with a width of more than 100 μm are used in order to drive external circuits. The standard low voltage (1.2 V) NMOS transistors can tolerate a TID value of up to 200 krad and have been used as is. The higher TID value an IC can withstand, the less metal shielding will be required in space, which in turn can reduce the weight of a satellite payload. For design of the SPI interface, a radhard digital library is available in the chosen semiconductor process. It includes logic components that experience no single-event latch-ups at a particle hit with a linear energy transfer (LET) value of up to 62 $MeVcm^2/mg$. Available triple modular redundancy flip-flops show no single-event upsets up to the same LET value of particle hits. From the architectural point of view, any kind of redundancy improves the radiation hardness of the circuit. Because of power consumption penalty, it cannot be used everywhere in the circuit. In this design, each of the TIA channels receives four controlled currents generated by a dedicated 4-channel DAC. In order to supply bias currents to the opamps, each TIA channel contains a separate bandgap voltage reference circuit. Such a redundant biasing scheme guarantees reliable

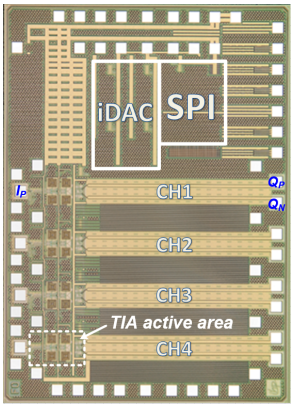

Fig. 3: Microphotograph of the TIA IC.

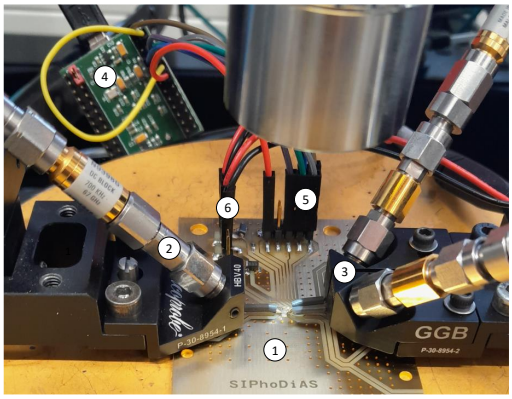

Fig. 4: HF probing of the TIA IC placed on a PCB.

operation of other channels in case if one channel operation is affected by a high energy particle strike.

IV. Electrical Characterization

The TIA IC was fabricated in the 130 nm SiGe BiCMOS technology featuring bipolar transistors with f_T/f_{MAX} values of 250/340 GHz, respectively. Fig. 3 shows a microphotograph of the chip. The active area of a single TIA core is 300 x 250 μm^2.

To determine the maximum data rate that can be delivered by the bare TIA IC, we perform a HF probing measurement. The probe setup is shown in Fig. 4. In order to apply power and SPI signals, the IC has been placed on the PCB. The power supply, DC, and SPI pads have been wirebonded. The SPI master controlled by a PC can provide appropriate programming of the on-chip SPI part.

The TIA ICs have been characterized in time domain by applying an input signal to one channel at a time through a HF probe and measuring an output signal over an HF probe connected by a cable to a sampling oscilloscope. As an input signal, we used a PRBS31 sequence for all tests. Fig. 5 shows the TIA output eye-diagrams at 2.5 V and 3.3 V supply. The operation from a 3.3 V supply is required for the optical transceiver module. In this mode, a clear eye diagram at 40 GS/s have been measured. This provides enough

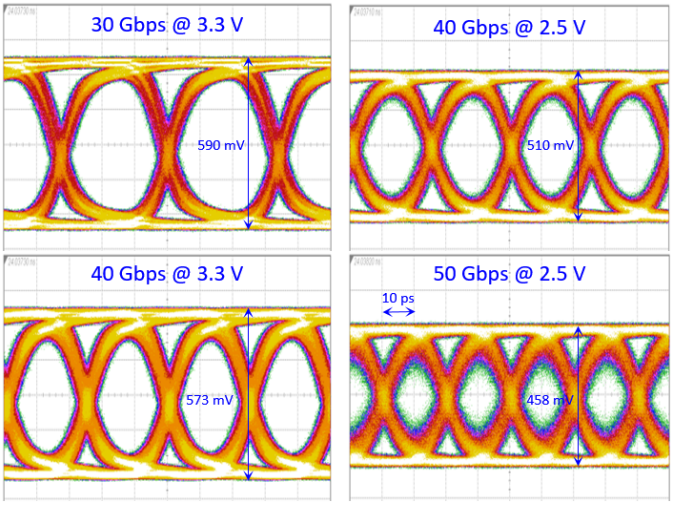

Fig. 5: Eye diagrams at different data rates and supply voltages.

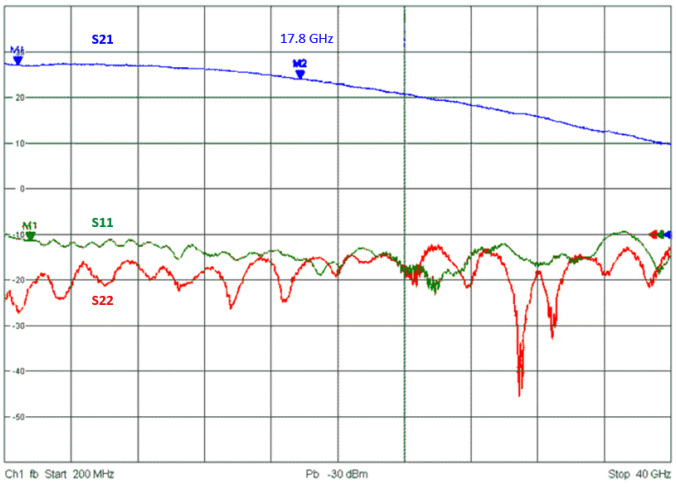

Fig. 6: S-parameter measurements at a power supply of 3 V. S_{11} – green; S_{22} – red; S_{21} – blue.

data rate margin in order to achieve the targeted 28 Gb/s per channel operation in the final optical transceiver assembly, even taking into account a photodiode that introduces 100 fF of capacitance at the TIA input. Showing a power consumption of 107.7 mW/ch, the TIA IC achieves an energy efficiency value of 3.85 pJ/bit at 28 Gb/s. To check the maximum possible energy efficiency, the TIA IC has been designed to operate at the supply voltages down to 2.5 V. After applying this voltage, the maximum possible data rate of 50 Gb/s has been demonstrated. At these conditions, the quad channel TIA IC demonstrates the maximum energy efficiency value at 1.35 pJ/bit. The extracted from measurements input referred noise of the TIA is 5.8 μA_{rms}.

For S-parameter measurements, the input port was set in a single-ended and output port in a differential configuration. Fig. 6 shows the measured S-parameters at default SPI register settings and at 3 V supply voltage. From the S_{21} curve, the TIA

TABLE I
ELECTRICAL PERFORMANCE COMPARISON OF TIAS IN NRZ MODE

Reference	Technology	f_T GHz	Transimpedance dBΩ	SE/S2D/Diff.	Number of channels	Data rate/channel Gb/s	P_{DC} mW/channel	Efficiency pJ/bit
[4]	130 nm BiCMOS	250	68.5	Diff.	Single	90	150	1.6
[4]	130 nm BiCMOS	300	65	Diff.	Single	100	150	1.5
[8]	22 nm CMOS	350	59	SE	Single	80	11.2	0.14
[9]	250 nm BiCMOS	180	80	Diff.	Quad	25	65	2.6
[10]	55 nm BiCMOS	320	65	Diff.	Quad	90	150	1.6
This work	130 nm BiCMOS	250	68.5	Diff.	Quad	50	67.5	1.35

IC shows a 3-dB bandwidth of 17.8 GHz. For both, input and differential output, the circuit demonstrates good performance in terms of reflection. The S_{11} and S_{22} parameters are below than -10 dB up to 40 GHz.

Table I compares the state-of-the-art TIA ICs with the current work. Our quad TIA IC presents the best energy efficiency compared to the other SiGe BiCMOS TIA IC realizations despite of covering wide operation range and radiation hardening. A single channel design in 22 nm CMOS [8] shows an order of magnitude better efficiency compared to this work. It offers a significant efficiency margin to implement single-ended-to-differential (S2D) operation, multi-channel functionality and bias control. Nevertheless, this work demonstrates proven radiation hardness and ability to deliver the output signal of more than 450 $mV_{pp\text{-}diff}$ to the 100 Ohm load.

V. IRRADIATION TESTS

The TIA IC underwent the irradiation testing for cumulative effects including TID and total non-ionizing dose (TNID). The TID test has been realized by gamma radiation test (Fig. 7). For this test, two PCBs carrying TIA IC have been exposed stepwise to 20, 50 and 100 krad ionization doses followed by two annealing steps (24 hours at 25°C and 168 hours at 100°C). This test was conducted in order to see the performance degradation that might be caused mostly by the CMOS devices. After performing all TID tests, the TIA circuits shown stable power consumption and correct SPI functionality.

TNID effects are caused by the non-ionizing transfer of energy, when the striking particle displaces atoms in the semiconductor lattice. This can cause a variety of effects in bipolar devices and optoelectronic components including photodetectors and laser diodes. The TNID test has been fulfilled by a flux of protons $5x10^{11}$ p/cm^2, having an energy of 60 MeV. Fig. 7 shows the corresponding measurement setup in the irradiation facility. For both TIA boards power consumption and eye diagrams before and after proton test have been measured. There were no visible changes in the eye diagrams.

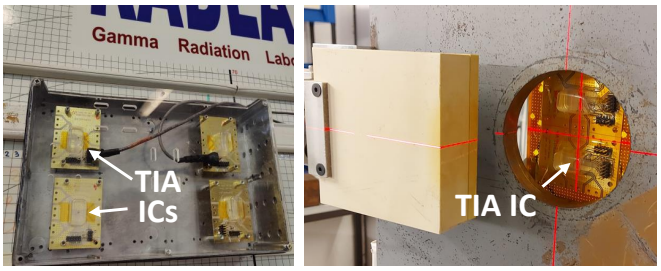

Fig. 7: Test setup for gamma radiation (left) and proton test (right).

The increase in DC current below 0.6 % was observed after irradiation.

VI. CONCLUSION

In this paper, we presented the quad TIA IC development, which contained many trade-offs in order to be compatible for an optical transceiver module in terms of electrical performance, form factor and operation in a harsh space environment. Energy efficiency was the main focus during the IC design. For that purpose, the circuit has been designed having high order of programmability by means of an SPI interface. At the same time, the IC design was conducted in a way to assure reliable operation within a wide power supply range from 2.5 to 3.3 V. For decreasing the interchannel crosstalk, an LDO has to be implemented in each TIA core, which leads to an increase of power supply and, consequently, power consumption. Nevertheless, having all these limitations, the TIA IC operating at 2.5 V supply demonstrated the best energy efficiency compared to the SiGe TIA realizations. At 3.3 V supply, TIA IC operation showed sufficient data rate margin to be utilized in a 28 Gb/s optical transceiver module. The radiation hardness was confirmed by conducting the gamma and proton irradiation tests.

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REFERENCES

[1] A. Le Pera, F. Forni, M. Grossi, M. Lucente *et al.*, "Digital transparent processor for satellite telecommunication services," in *Proc. IEEE Aerospace Conf.*, 2007, pp. 1–9.

[2] L. Cyrille, N. Venet, C. Vo Van, N. Nicolas *et al.*, "Optical interconnect evaluation process for Thales Alenia Space latest generation of digital transparent processor, DTP6G, and a projection into future needs," in *Proc. SPIE 12777, International Conference on Space Optics (ICSO)*.

[3] S. Giannakopoulos, I. Sourikopoulos, L. Stampoulidis, P. Ostrovskyy *et al.*, "A 112 Gb/s radiation-hardened mid-board optical transceiver in 130-nm SiGe BiCMOS for intra-satellite links," *Frontiers in Physics*, vol. 9, pp. 1–16, May 2021.

[4] I. G. Lopez, A. Awny, P. Rito, M. Ko *et al.*, "100 Gb/s Differential Linear TIAs With Less Than 10 pA/$\sqrt{\text{Hz}}$ in 130-nm SiGe:C BiCMOS," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 2, pp. 458–469, Feb. 2018.

[5] M. Krstic, J. Schmidt, A. Breitenreiter, F. Teply *et al.*, "Evaluierung einer strahlungsharten Bibliothek in 0.13μm BiCMOS," in *Proc. DLR Bauteile Konferenz*, 2018.

[6] J. D. Cressler, "SiGe HBT technology: a new contender for Si-based RF and microwave circuit applications," *IEEE Trans. on Microwave Theory and Techniques*, vol. 46, no. 5, pp. 572–589, May 1998.

[7] P. Ostrovsky, O. Schrape, K. Tittelbach-Helmrich, F. Herzel *et al.*, "A radiation hardened 16 GS/s arbitrary waveform generator IC for a submillimeter wave chirp-transform spectrometer," in *Proc. IEEE Nordic Circ. and Syst. Conf. (NORCAS)*, Oct. 2018, pp. 1–4.

[8] S. Daneshgar, H. Li, T. Kim, and G. Balamurugan, "A 128 Gb/s PAM4 linear TIA with 12.6 pA/$\sqrt{Hz}$ noise density in 22 nm FinFET CMOS," in *Proc. IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Jun. 2021, pp. 135–138.

[9] M. Ko, K. Tittelbach-Helmrich, V. Petrovic, and D. Kissinger, "25-Gb/s/Channel VCSEL driver and transimpedance amplifier array ICs in 0.25μm SiGe:C BiCMOS technology for Space Applications," in *Proc. 6th International Workshop on Analogue and Mixed-Signal Integrated Circuits for Space Applications (AMICSA)*, 2016.

[10] J. Lambrecht, H. Ramon, B. Moeneclaey, J. Verbist *et al.*, "90-Gb/s NRZ optical receiver in silicon using a fully differential transimpedance amplifier," *Journal of Lightwave Technology*, vol. 37, no. 9, pp. 1964–1973, May 2019.