A 196-MHz Bandwidth Transimpedance Amplifier with High Out-of-Band Rejection Employing Transmission Zeros

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***Abstract*—This paper presents a baseband Rauch transimpedance amplifier (TIA) topology with 196-MHz bandwidth (BW) for Sub-7-GHz direct-conversion receivers (RXs). By connecting an equivalent RLC bypass network in parallel, a pair of transmission zeros around the channel bandwidth is introduced to achieve out-of-band (OOB) rapid roll-off while effectively suppressing close-in blockers. To meet the TIA's requirements for high bandwidth and excellent in-band (IB) and out-of-band (OOB) linearity, the circuit incorporates a three-stage operational transconductance amplifier (OTA) to achieve high DC gain and gain–bandwidth product (GBW). Designed in 28-nm CMOS technology, the circuit occupies a 0.05-mm^2 area and consumes 22.5 mW of power from a 1-V supply voltage. The TIA achieves a 196-MHz baseband bandwidth, an OOB rejection of 24 dB at 3-baseband-bandwidth (BB-BW), an adjacent-channel OOB IIP3 of 46.9 dBm at 2-BB-BW, and an integrated input-referred noise (IRN) of 147.5 μVrms from 1-MHz to 196-MHz. The corresponding FoM value reaches 186.5 dBJ^{-1}, surpassing all previous designs.**

Keywords—Rauch transimpedance amplifier, transmission zeros, three-stage operational transconductance amplifier (OTA), wide bandwidth, out-of-band (OOB) Rejection, linearity.

I. Introduction

With advances in wireless communication technology, driven by user market demands for higher data transmission rates, lower latency, and denser terminal connection densities, the radio frequency channel bandwidth (BW_{RF}) has progressively increased. However, the relative frequency offset ($\Delta f_{Blocker}$) of blocking signals remains constant, resulting in a continuous decline in the $f_{Blocker}/BW_{RF}$ ratio. Consequently, wireless receivers (RXs) have to deliver sufficiently steep out-of-band roll-off characteristics and exceptional linearity to prevent strong adjacent-band signals from interfering with their normal operation.

Transimpedance amplifiers (TIAs) have been frequently employed within the baseband modules of current-mode receivers. In the case of insufficient RF filtering, TIAs may encounter high-power out-of-band interference sources during signal processing. The conventional TIA topology performs current-to-voltage signal conversion, offering only a first-order roll-off characteristic [1]–[4]. By removing the negative feedback capacitor and introducing a load capacitor at the TIA output, a second-order filtering effect can be achieved [5]. However, this would result in the loss of the compensating zero generated by the feedback capacitor, thereby degrading differential-mode (DM) loop stability.

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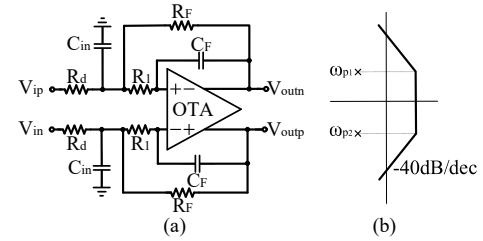


Fig. 1. (a) Conventional Rauch TIA topology. (b) S-plane and zero-pole.

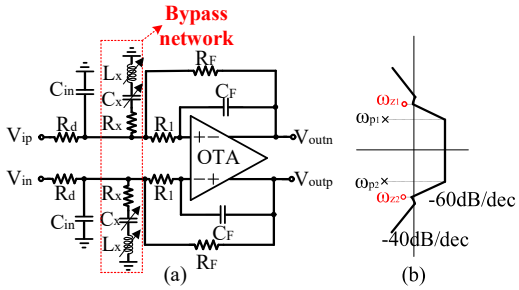
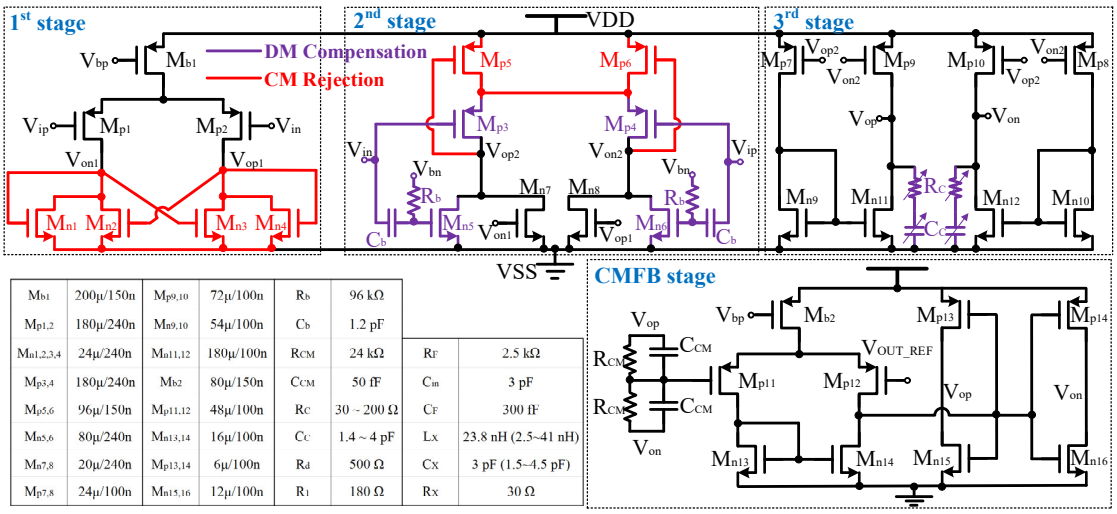


Fig. 2. (a) Proposed Rauch TIA topology. (b) S-plane and zero-pole.

The Rauch TIA [6] and its modified structures [7], [8] have been extensively studied owing to their second-order and higher-order roll-off characteristics. C. Tao ingeniously achieved third-order characteristics by employing the intermediate node of the RC compensation as the output terminal [7], yet this approach failed to improve out-of-band (OOB) linearity. M. A. Montazerolghaem introduced a high-pass impedance into the feedback network to achieve equivalent third-order filtering [8]. However, this method degraded the phase margin of the differential-mode loop.

Moreover, situated at the end of the RX front-end signal chain, the overall linearity of the receiver is predominantly constrained by the TIA in most scenarios. To achieve exceptional in-band (IB) and out-of-band (OOB) linearity, researchers primarily employs two-stage [3] and three-stage [1], [2], [4], [6], [7], [8] operational transconductance amplifiers (OTAs), thereby attaining an exceptionally high DC gain and gain-bandwidth product (GBW). The latter typically exhibits superior linearity but presents challenges in loop stability.

This paper proposes a transmission zero technique to achieve rapid out-of-band roll-off, while simultaneously enhancing out-of-band linearity with negligible impact on loop stability. Section II details the theoretical derivation and circuit design, Section III presents the layout and post-simulation results, and Section IV draws conclusions.



M_{b1}	200μ/150n	$M_{p9,10}$	72μ/100n	R_b	96 kΩ		
$M_{p1,2}$	180μ/240n	$M_{n9,10}$	54μ/100n	C_b	1.2 pF		
$M_{n1,2,3,4}$	24μ/240n	$M_{n11,12}$	180μ/100n	R_{CM}	24 kΩ	R_F	2.5 kΩ
$M_{p3,4}$	180μ/240n	M_{b2}	80μ/150n	C_{CM}	50 fF	C_{in}	3 pF
$M_{p5,6}$	96μ/150n	$M_{p11,12}$	48μ/100n	R_C	30 ~ 200 Ω	C_F	300 fF
$M_{n5,6}$	80μ/240n	$M_{n13,14}$	16μ/100n	C_C	1.4 ~ 4 pF	L_X	23.8 nH (2.5~41 nH)
$M_{n7,8}$	20μ/240n	$M_{p13,14}$	6μ/100n	R_d	500 Ω	C_X	3 pF (1.5~4.5 pF)
$M_{p7,8}$	24μ/100n	$M_{n15,16}$	12μ/100n	R_1	180 Ω	R_X	30 Ω

Fig. 3. The proposed three-stage differential OTA circuit.

II. Circuit Design and Analysis

A. Proposed Rauch TIA Topology

The conventional Rauch TIA circuit topology, as depicted in Fig. 1(a), incorporates R_1 at the input to form a pair of conjugate complex poles, thereby achieving a second-order roll-off characteristic, as shown in Fig. 1(b). The TIA's transfer function can be obtained as

$$A_{v1}(s) = \frac{V_{out}}{V_{in}} = -\frac{\frac{R_F}{R_d}}{s^2\,(R_F\,C_F\,R_1\,C_{in}) + sC_F\left(R_F + R_1 + \frac{R_F\,R_1}{R_d}\right) + 1} \quad (1)$$

The pair of conjugate complex poles can be expressed as

$$\omega_{P1,2} = \frac{-C_F\left(R_F + R_1 + \frac{R_F\,R_1}{R_d}\right) \pm i\sqrt{4R_FC_FR_1C_{in} - C_F\left(R_F + R_1 + \frac{R_F\,R_1}{R_d}\right)}}{2\,R_F\,C_F\,R_1\,C_{in}} \quad (2)$$

where R_F is the feedback resistor, R_d is the preceding mixer's equivalent resistance, C_{in} is the parallel capacitance of the input node, C_F represents the feedback capacitance, and R_1 is the resistor introduced to achieve second-order filtering characteristics. The ratio of the feedback resistor R_F to the mixer's equivalent resistance R_d determines the DC-gain. The bandwidth is jointly determined by all resistors and capacitors.

The proposed novel TIA circuit is illustrated in Fig. 2(a). By connecting a bypass network composed of the RLC series circuit in parallel at the input node, a new transfer function is formed as

$$A_{v2}(s) = -\frac{R_F}{R_d} \times \frac{C_xL_xS^2 + C_xR_xS + 1}{AS^4 + BS^3 + CS^2 + DS + 1} \quad (3)$$

$$A = R_FC_FR_1C_{in}C_xL_x$$

$$B = C_FC_x\,[R_FR_1C_{in}R_x + (R_F + R_1 + \frac{R_FR_1}{R_d})L_x]$$

$$C = C_FR_FR_1(C_{in} + C_x) + C_FC_xR_x\left(R_F + R_1 + \frac{R_F\,R_1}{R_d}\right) + C_xL_x$$

$$D = C_F\left(R_F + R_1 + \frac{R_F\,R_1}{R_d}\right) + C_xR_x$$

where R_x, L_x, and C_x are the values of the RLC components within the bypass network, respectively.

The transfer function possesses two pairs of conjugate complex poles and one pair of newly introduced transmission zeros. The zeros can be expressed as

$$\omega_{Z1,2} = \frac{-R_xC_x \pm i\sqrt{4\,C_x\,L_x - (C_xR_x)^2}}{2\,C_x\,L_x} \quad (4)$$

It can be known from (3) and (4) that introducing complex zeros with an extremely small real part has brought the numerator of the transfer function to decay sharply near the imaginary frequency of the zeros. This manifests as steep attenuation on the amplitude-frequency response curve, thereby achieving rapid out-of-band roll-off, akin to the action of a notch filter, as shown in Fig. 2(b).

B. Differential OTA Implementation

The key to TIA's design lies in the internal operational transconductance amplifier (OTA). To achieve superior in-band and out-of-band linearity, a three-stage differential OTA is adopted while attaining exceptionally high DC gain and GBW, as shown in Fig. 3.

To stabilize the differential-mode (DM) loop of the three-stage OTA, the proposed circuit employs feedforward compensation and RC zero compensation. The feedforward compensation path is situated between the input of the first stage and the output of the second stage, while the RC compensation is positioned at the output node of the third stage, V_{O+}/V_{O-}. Both compensation methods can introduce the left-half-plane (LHP) zeros, thereby compensating for the phase margin. The expressions for two LHP zeros are as follows:

$$\omega_{Zero1} = -\left(\frac{g_{m1}\,g_{m2}}{g_{mf}\,C_{o1}} + \frac{1}{r_{o1}C_{o1}}\right) \quad (5)$$

$$\omega_{Zero2} = -\frac{1}{R_c\,C_c} \quad (6)$$

where g_{m1}, g_{m2}, and g_{mf} are the transconductance of the first stage, second stage, and feedforward compensation stage, respectively. C_{o1} and r_{o1} are the load capacitance and output resistor of the first stage. R_C and C_C represent the resistor and capacitor for zero compensation.

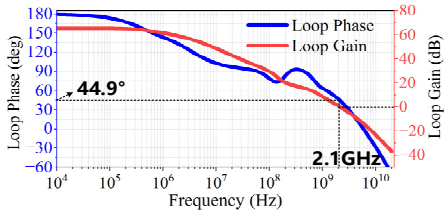


Fig. 4. Post-simulated frequency response of the proposed TIA's DM loop.

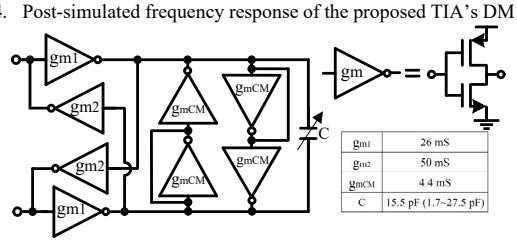


Fig. 5. Active inductor circuit.

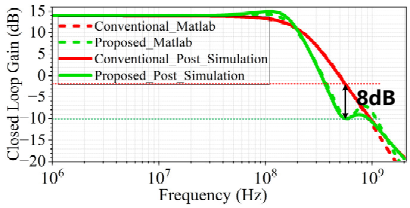


Fig. 6. Closed-loop gain response of the conventional and proposed TIAs from MATLAB simulation and post-simulation of the circuit.

The Bode plots for the DM loop are shown in Fig. 4, exhibiting a phase margin of 44.9° and a GBW of 2.1 GHz. Regarding the stability of the common-mode (CM) loop, the proposed OTA employs a local common-mode feedback (CMFB) circuit. Furthermore, its first and second-stage amplification circuits adopt a CM low-output impedance and DM high-output impedance structure to suppress CM loop gain. For instance, in the second-stage amplification circuit, the CM output impedance $1/g_{mp5,6}$ is 48 Ω, while the DM output impedance $r_{on5,6} // r_{on7,8} // (g_{mp3,4} r_{op3,4} r_{op5,6})$ is about 2.6 kΩ, where g_m and r_o are the transconductance and small-signal output resistance of the MOS transistor, respectively. Then we obtain the high gain of DM and the low gain of CM.

C. Active Inductor

From (4), to achieve the imaginary part of zeros equal to 3-BB-BW (about 600 MHz), which is the desired notch point, when $C_X = 3$ pF and $R_X = 30$ Ω, we can calculate that $L_X = 22.8$ nH. Coupling such a large inductance via on-chip passive coils would occupy an unacceptably large area, rendering it virtually unfeasible. Therefore, an active inductance is designed by transposing the impedance of the capacitor via a gyrator, as illustrated in Fig. 5. As there is only one equivalent active inductance in the circuit, which is used for two L_X in series, the equivalent value of the active inductance can be expressed as

$$L_{total} = \frac{4\,C}{g_{m1}\,g_{m2}} = 2\,L_x \tag{7}$$

where C denotes the capacitor used for impedance transformation in the gyrator, its capacitance ranges from 1.7 pF to 27.5 pF, with a nominal value of 15.5 pF. To enhance robustness against PVT variations, capacitor C is implemented as a digitally programmable capacitor array to achieve the required equivalent inductance. gm1 and gm2 are the transconductance values of the transconductance block, 26 mS and 50 mS, respectively. The calculated equivalent inductance, LX, is 23.8 nH, which is essentially consistent with our earlier estimated value of 22.8 nH.

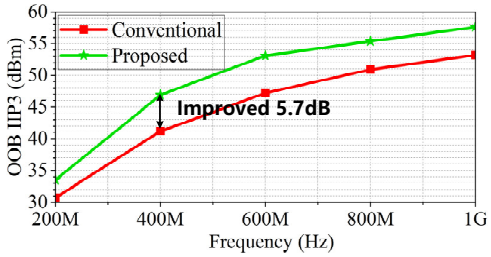


Fig. 7. Comparion of OOB-IIP3 post-simulation of Rauch TIA.

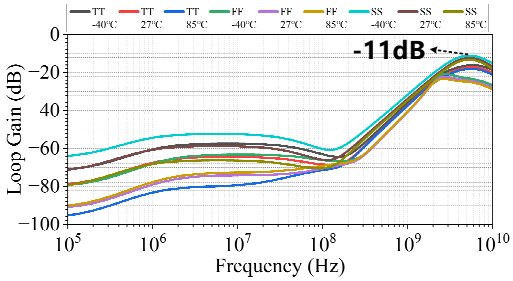


Fig. 8. Common mode loop gain under PVT post-simulation.

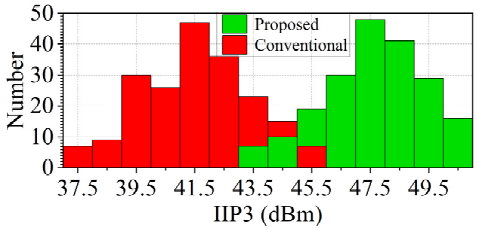


Fig. 9. Post-simulated OOB-IIP3 with two tones of 400 MHz and 770 MHz (Monte Carlo with 200 samples).

TABLE I. TIA CORNER STABILITY OF DIFFERENTIAL-MODE

Corner	TT			SS			FF		
Temperature[°C]	-40	27	85	-40	27	85	-40	27	85
GBW [GHz]	2.5	2.1	2	2.2	1.9	1.7	1.9	1.6	1.5
PM [deg]	39	45	47	45	49	53	38	41	43

D. OOB Rejection and Linearity

To verify the consistency between the aforementioned theoretical derivation and actual TIA circuit behavior, we compare MATLAB simulation results with post-simulation results. As can be seen from Fig. 6, the amplitude-frequency characteristic curves indicate that the proposed transmission zero technique performs in circuit simulations as theoretically anticipated. Compared to the conventional Rauch TIA, the proposed Rauch TIA topology achieves an additional 8 dB of OOB suppression at the 3-BB-BW. Moreover, owing to the low impedance of the bypass network near the imaginary part of the transmission zero, the proposed TIA exhibits a 5.7-dB improvement of OOB-IIP3 compared to conventional structures, as illustrated in Fig. 7.

E. Robustness

To validate the robustness of the proposed TIA circuit, the phase margin of the CM and DM loops under various PVT conditions is simulated. As shown in Fig. 8, the loop gain of CM remains below –11 dB across all process corners, thereby eliminating the risk of CM oscillation. The phase margin of the DM loop, as detailed in TABLE I, ranges from 38° to 53°, indicating favorable stability.

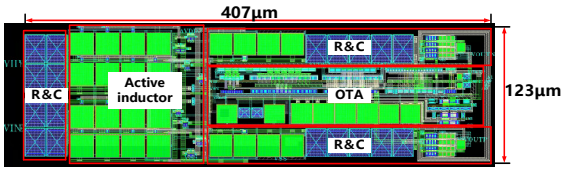


Fig. 10. Layout of the proposed TIA.

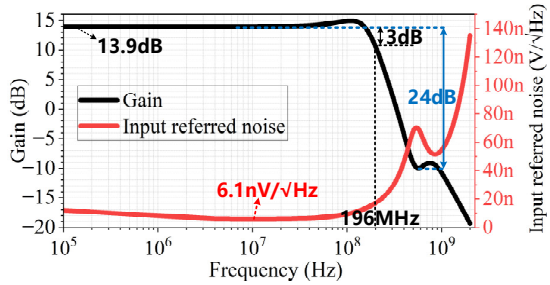


Fig. 11. Post-simulated closed-loop frequency response and input-referred noise.

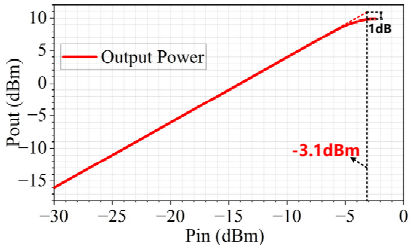


Fig. 12. Post-simulated P-1dB.

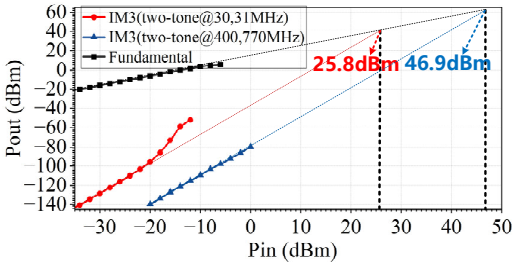


Fig. 13. Post-simulated in-band IIP3 with two tones of 31 MHz and 32 MHz and out-of-band IIP3 with two tones of 400 MHz and 770 MHz.

Additionally, the paper presents the results of OOB IIP3 under Monte Carlo post-simulation, as shown in Fig. 9. It is noted that the proposed transmission zeros technique delivers a relatively stable improvement for OOB IIP3.

III. Post-Layout Simulation Results

The proposed TIA is designed in 28-nm CMOS. As shown in Fig. 10, the layout area of the core circuit is 0.05 mm^2. The design operates under a supply voltage of 1 V with a total power dissipation of 22.5 mW. The OTA and active inductor circuits consume 15.3mW and 7.2mW, respectively. The closed-loop frequency response and input-referred noise are given in Fig. 11. The DC gain is 13.9 dB with a bandwidth of 196 MHz, and it exhibits a third-order roll-off characteristic beyond the passband down to 600 MHz, after which it reverts to second-order filtering. The input-referred equivalent noise (IRN) integrated from 1 MHz to 196 MHz is 147.5 $\mu V/\sqrt{Hz}$. Among these, active inductors account for less than 0.4% of the total input-referred noise. According to Fig. 12, the 1 dB compression point (P-1dB) is –3.1 dBm, essentially achieving rail-to-rail output from VDD to VSS.

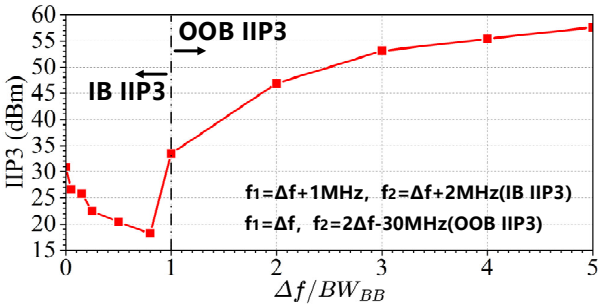


Fig. 14. Post-simulated IIP3 versus frequency.

TABLE II. Performance Summary and Comparison

Parameter	This Work[a]	JSSC' 18 [1]	ISCAS' 23 [2][a]	TCAS-I' 20 [6]
Process [nm]	28	28	40	65
Filter order [N]	3	1	1	2
Fc (BW) [MHz]	**196**	20	50	80
Gain [dB]	13.9	14	14	14
OOB Rejection[b] [dB]	**24**	11	11	12
IB IIP3 [dBm]	25.8	31.5	31.6	19.4
OOB IIP3[c] [dBm]	**46.9**	42	41	26.8
f_{IM3} [MHz]	30	10	30	10
IRN[d] [uV_{RMS}]	33.4	16.7	22.3	17.6
SFDR[e] [dB]	82.3	83	80.7	72.6
Supply [V]	1	1.8	1.2	1.8
Power consumption [mW]	22.5	5.4	10.4	14.2
Area [mm^2]	0.05	0.026	0.016	0.037
FoM[f] [dB]	**186.5**	178.7	177.5	173.1
FoM_{IM3}[g] [dB]	**178.3**	175.7	175.3	164.1

[a] Post-layout simulation results. [b] = DC gain – gain (@f=3×BW). [c] Two-tones (f_1=BW, f_2=2×BW–f_{IM3}). [d] IRN is normalized to 10MHz, assuming thermal noise is dominant. [e] SFDR=10 lg $(\frac{OOB\ IIP3}{P_{IRN}})^{\frac{2}{3}}$. [f] FoM=SFDR+10 lg $(\frac{BW \cdot N}{Power})$. [g] FoM_{IM3}=FoM+10 lg $(\frac{f_{IM3}}{BW})$

In the IIP3 simulation shown in Fig. 13, the in-band IIP3 is 25.8 dBm with two tones of 31 MHz and 32 MHz, while the out-of-band IIP3 is 46.9 dBm with two tones of 400 MHz and 770 MHz. Fig. 14 illustrates the variation trend of IIP3 from in-band (IB) to out-of-band (OOB). As frequency increases, IIP3 gradually decreases within the band, then begins to rise in the out-of-band region. The reduction of IB-IIP3 is primarily constrained by the GBW of internal OTA, while the improvement of OOB-IIP3 correlates with filter characteristics. The complete performances are summarized in TABLE II, where the proposed circuit demonstrates better performances in terms of the Figure of Merit (FOM).

IV. Conclusion

This paper presents a novel Rauch TIA featuring high out-of-band roll-off characteristics, achieved by introducing transmission zeros via a bypass RLC network. The internal three-stage OTA employs feedforward compensation and RC zero compensation to achieve DM loop stability, while maintaining CM loop gain consistently below -11 dB through local CMFB and CM rejection amplification stages. The proposed TIA is designed in 28-nm CMOS process, consuming 22.5-mW from 1-V supply voltage. It simultaneously achieves a 196-MHz bandwidth, third-order out-of-band filtering characteristics, and an exceptional adjacent-channel OOB IIP3 of 46.9 dBm.

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