A 50/25/12.5 Gb/s Fast-Settling Burst-Mode Transimpedance Amplifier for 50G-PON

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***Abstract*—This paper presents a reconfigurable burst-mode (BM) transimpedance amplifier (TIA), supporting triple rates of 50/25/12.5-Gb/s for both symmetrical and asymmetrical 50G-PON. Triple rate bandwidth scaling gain modes are adopted in high-gain (HG) mode while a merged bandwidth gain mode is utilized in low-gain (LG) mode. For rapid settling, a concurrent offset cancellation (OC) scheme is implemented to activate AOC and ROC loops in parallel, eliminating the cumulative delay inherent in sequential loop activation. In HG mode, the TIA achieves simulated gains of 82/85/86 dBΩ with corresponding 3-dB bandwidths of 38/13/7 GHz for 50/25/12.5 Gb/s rate, respectively. Meanwhile, in LG mode, it provides a gain of 61.5 dBΩ while extending the bandwidth to 42 GHz. Finally, the TIA achieves a record burst-mode settling time of 6.5 ns.**

Keywords—50G-PON, burst-mode, TIA, fast-settling, offset cancelation

I. Introduction

With the explosive growth of 5G communications, cloud computing, high-definition video services and AI, the large-scale commercialization of 10-Gigabit-capable passive optical networks (PON) is imminent. Currently, the 50G-PON standard explicitly defines various data rate configurations, supporting both symmetric and asymmetric transmission. Specifically, the downlink rate is fixed at 50 Gb/s, while the uplink supports three selectable line rates: 12.5 Gb/s, 25 Gb/s, and 50 Gb/s in burst-mode. As illustrated in Fig. 1, the design of a burst-mode transimpedance amplifier (BM-TIA) for 50G-PON faces three primary technical challenges: (1) As a critical front-end component in optical receivers, the TIA must achieve high bandwidth and low equivalent input noise to ensure high transmission rates and superior sensitivity. (2) Supporting multi-rate scenarios has become essential to minimize deployment costs and enhance network flexibility. (3) The time-division multiplexing (TDM) burst-mode communication used in 50G-PON necessitates that the TIA achieves rapid settling for automatic gain control (AGC) and offset cancellation (OC), etc.

A 25-Gbaud PAM-4 burst-mode receiver in 250-nm SiGe [1] achieved offset elimination through integrated AGC and AOC loops, reaching an 82.7-ns settling time and 15.8-dB dynamic range. However, conventional loops often face inherent speed limitations. Although digital-loop approaches [2] significantly accelerate response times, they typically incur high power consumption and limited dynamic range. Another 28-nm CMOS receiver [3] utilized integrate-and-dump and amplitude comparators to extract signal information within two UIs, achieving a 2.24-ns settling time but with a limited 5-dB dynamic range. Balancing ultra-fast settling with optimized overall performance remains a critical challenge. To address this, this paper proposes a 50/25/12.5 Gb/s triple-rate BM-TIA in 90-nm SiGe, optimized for low parasitics and rapid transient response.

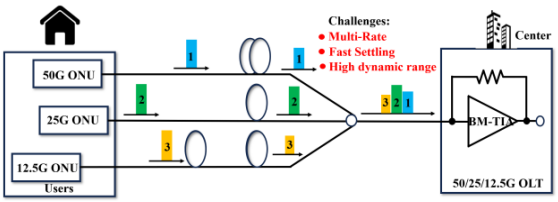


Fig. 1. The challenges faced by BM-TIA.

The rest of this paper is organized as follows: Section II describes the proposed BM-TIA architecture and its RF signal path, providing a detailed analysis of the circuit implementation and its multi-rate operational principles. Section III presents the post-layout simulation results, showing the effectiveness of the accelerated AOC/ROC loops in minimizing settling time. Furthermore, performance trade-offs regarding gain, noise, and response speed are discussed. Finally, Section IV concludes the paper.

II. Architecture And Circuit Implementation

The proposed BM-TIA architecture comprises two functional paths: the RF signal path, which is optimized for high bandwidth and low noise performance, and the burst-mode control path, designed specifically to facilitate rapid settling and transient response.

As illustrated in Fig. 2(a), the RF signal path comprises the front-end TIA (FE-TIA), a residual offset canceller (ROC), a single-ended-to-differential (S2D) converter, a variable gain amplifier (VGA), and an output buffer. As the critical front-end component, the TIA's noise performance directly dictates the overall receiver sensitivity. To optimize this, a two-pronged strategy is employed. From a topological perspective, we adopt a low-bandwidth FE-TIA combined with post-equalization, an approach proven to suppress integrated noise [5]. At the circuit level, a large feedback resistor and a cascode topology are utilized to further minimize thermal and shot noise contributions, as shown in Fig. 4(a). To ensure optimal sensitivity across all three data rates, high-gain modes are specifically optimized. Since bandwidth extension is primarily required for 50-Gb/s operation, the VGA is designed to provide active peaking only at high frequencies. This strategy significantly extends the bandwidth for the 50G mode while maintaining low complexity and minimizing parasitic loading for lower data rates. Additionally, the burst-mode section integrates the AOC, AGC, and the corresponding control logic (CTRL).

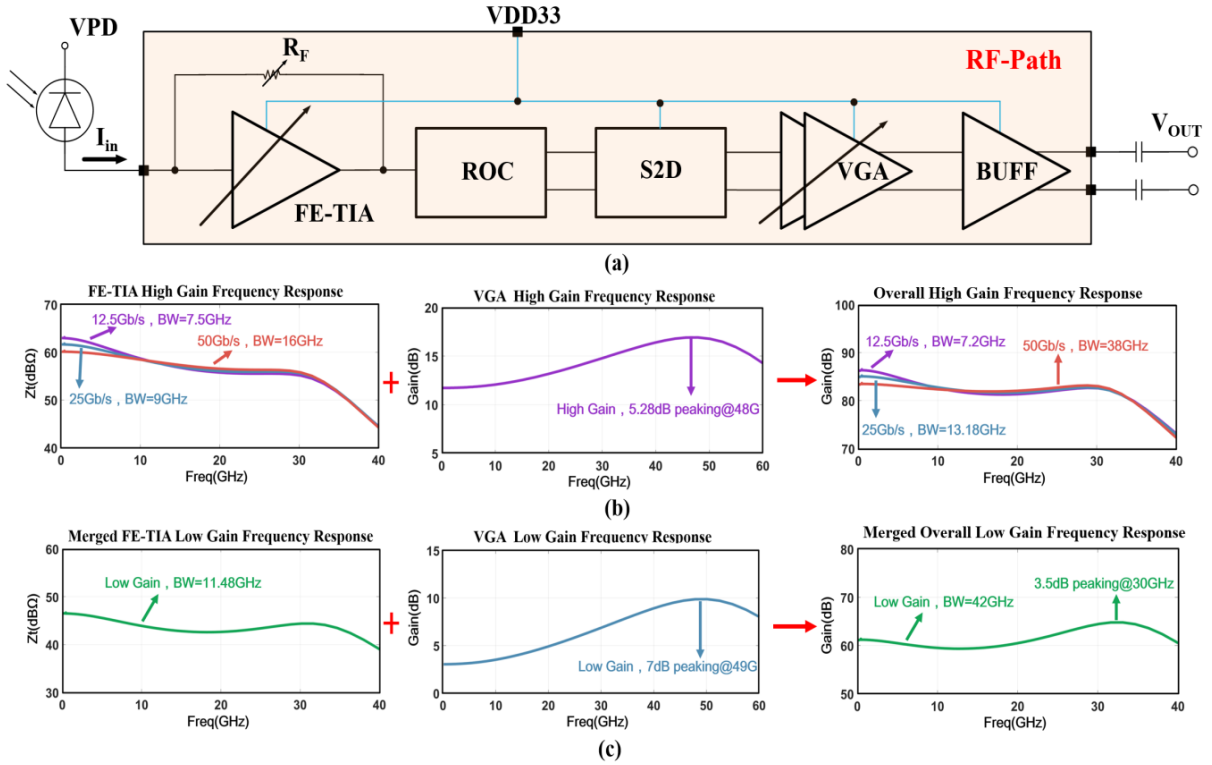


Fig. 2. (a) The RF path of BM-TIA. (b) High Gain Frequency Response. (c) Low Gain Frequency Response.

	BW Before Merger(Hz)	BW After Merger(Hz)
50G HG	30G	38G
25G HG	10G	13G
12.5G HG	5G	7G

(a)

	SNR
50G LG	49.26
25G LG	65.79
12.5G LG	78.12

Enough to meet BER requirements

(b)

HG Mode	LG Mode
50G HG	50G LG
25G HG	25G LG
12.5G HG	12.5G LG

HG Mode	LG Mode
50G HG	50G LG
25G HG	
12.5G HG	

(c)

Fig. 3. (a) Multi-rate bandwidth before and after the merger. (b) Signal-to-noise ratio at low gain before merger. (c) Low-gain mode multi-rate merger.

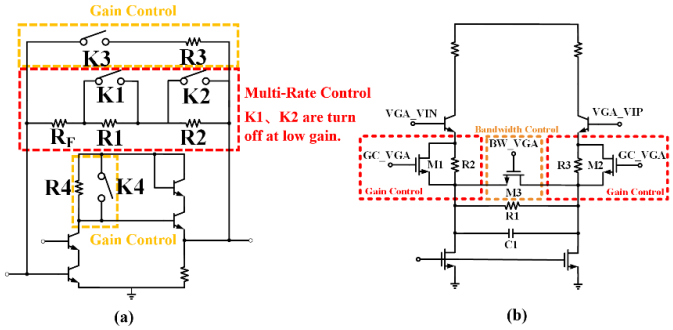
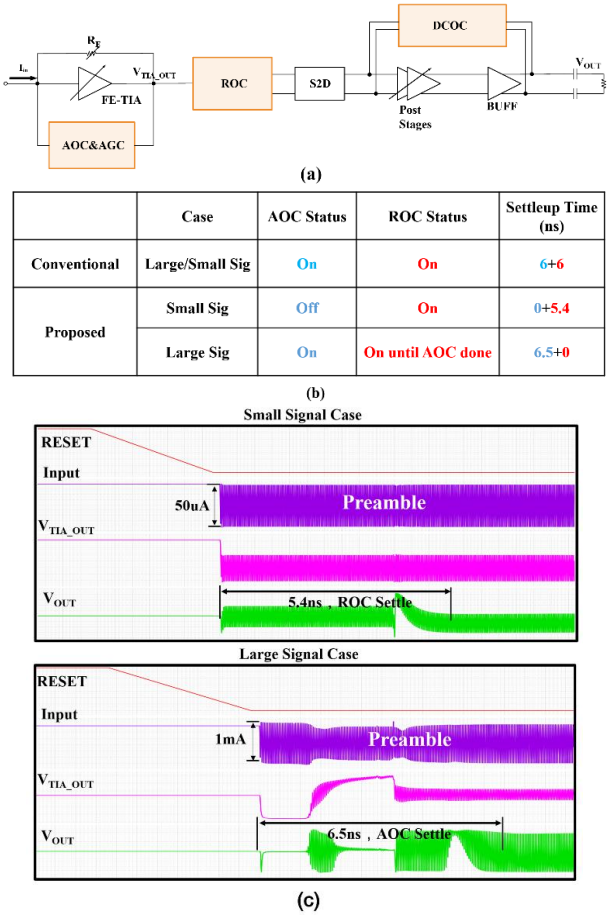


Fig. 4. Schematic of (a) Multi-rate TIA, (b) VGA cell.

A. Multi-rate TIA and VGA Design

To accommodate a wide dynamic range, the proposed multi-rate TIA and VGA operate in two distinct gain modes: high-gain (HG) and low-gain (LG). The 50G-PON standard's requirement for triple-rate (50/25/12.5-Gb/s) support typically necessitates six discrete gain configurations. As illustrated in Fig. 3(a), such an approach significantly increases design complexity and introduces substantial parasitic capacitance, which will degrade RF performance. To mitigate these issues, we propose a merged approach for low-gain. In HG mode, bandwidth is specifically customized for each data rate to maximize the signal-to-noise ratio (SNR). However, as shown in Fig. 3(b), the SNR for large signals within the LG mode's dynamic range significantly exceeds the bit-error-rate (BER) threshold of 1e-12. Consequently, a unified LG mode is implemented across all data rates in Fig. 3(c), eliminating the need for rate-specific bandwidth tuning in this mode. This strategy reduces parasitic capacitance by 20% and extends the TIA bandwidth from 35 GHz to 42 GHz at HG.

As illustrated in Fig. 4(a), the FE-TIA employs switches K1 to K4 for reconfiguration, thereby tailoring the bandwidth for different data rates [11]. In the 50-Gb/s mode, both K1 and K2 are turned off. The FE-TIA transitions to 25-Gb/s mode when K1 is conducting and K2 is open, and enters 12.5-Gb/s mode when both switches are closed. In the low-gain configuration, switch K3 adjusts the FE-TIA gain, while R4 is simultaneously reduced by close K4 to lower the open-loop amplifier gain to maintain loop stability. As shown in Fig. 4(b), the VGA utilizes three MOS switches (M1-M3) to concurrently tune the gain and bandwidth for high- and low-gain operations. The combined adjustment effects of the TIA and VGA are depicted in Fig. 2(b) for the high-gain mode and Fig. 2(c) for the low-gain mode, respectively .



	Case	AOC Status	ROC Status	Settleup Time (ns)
Conventional	Large/Small Sig	On	On	6+6
Proposed	Small Sig	Off	On	0+5.4
	Large Sig	On	On until AOC done	6.5+0

Fig. 5. (a) Burst topology diagram. (b) Burst mode working status. (c) Simulated burst mode response for small and large signal case.

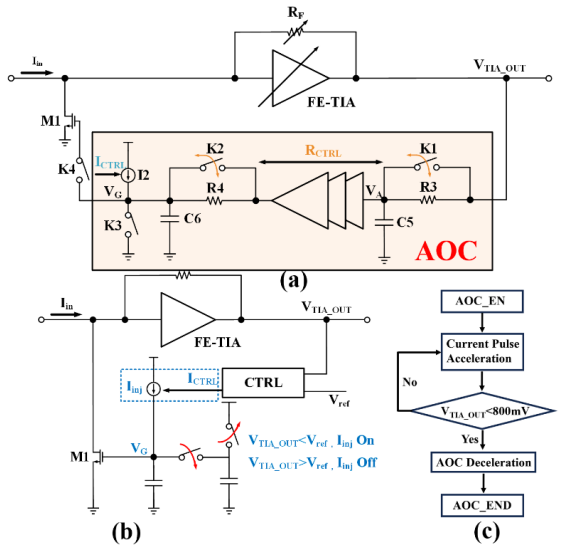


Fig. 6. (a)AOC schematic. (b) The principle of AOC. (c) AOC workflow chart.

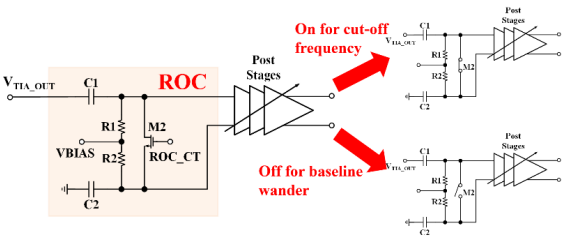


Fig. 7. ROC schematic diagram and working principle.

B. *Offset Cancellation Topology*

As illustrated in Fig. 5, conventional offset cancellation schemes typically employ a serial AOC-ROC process where the ROC only initiates after the AOC is complete [9]. Consequently, the total settling time is the sum of both processes. In this paper, we propose a control mechanism that utilizes the internal circuit states to generate control signals, significantly shortening the BM-TIA's settling time. When the input signal is near the sensitivity level, the TIA output offset remains small, allowing the AOC loop to be deactivated to prevent noise injection. In this scenario, the ROC eliminates the residual offset within 5.4 ns. Thus, the overall system settling time is primarily determined by the ROC's stabilization period, rather than the cumulative delay of a serial process.

When the input signal significantly exceeds the sensitivity level and the DC offset surpasses 50 mV, the AOC circuit is activated to suppress the large DC current. In this scenario, the AOC and ROC loops operate simultaneously. Unlike CMOS-based designs, the SiGe process exhibits a higher tolerance for residual offset owing to its higher supply voltage, which provides a larger voltage headroom that prevents internal nodes from early saturation. Consequently, once the AOC loop stabilizes, the remaining offset has a negligible impact on eye-diagram quality, allowing the ROC's effective elimination time to be significantly advanced. The AOC reaches stability within 6.5 ns, reducing the residual offset to less than 10 mV. Under these conditions, the overall system settling time is determined by the AOC's stabilization period. By leveraging this mechanism based on the circuit's internal state, the system setup time is reduced by 2× compared to conventional serial control methods.

C. *FE-TIA Offset Cancelation Loop Design*

As shown in Fig. 6, the AOC system comprises an amplification stage, a starter, an accelerator, and a reducer. By monitoring the DC offset at V_{TIA_OUT}, the AOC starter enables the circuit only when necessary. The accelerator employs a reconfigurable feedback loop: a small time constant facilitates rapid settling during the preamble, while a large time constant suppresses baseline drift during data transmission. To further expedite response beyond conventional techniques, this paper introduces a pulse-current acceleration mechanism. Unlike the constant-current charging used in [10], our approach achieves over an order-of-magnitude reduction in settling time compared to non-accelerated operations.

D. *VGA Offset Cancelation Loop Design*

As shown in Fig. 7, a switch is placed between the differential signal after the ac coupling capacitor C1/C2 as ROC, which shorts the two terminal during the process of the AOC establishment to suppress the FE-TIA offset and turns off when the payload data arrives to suppress the baseline drift.

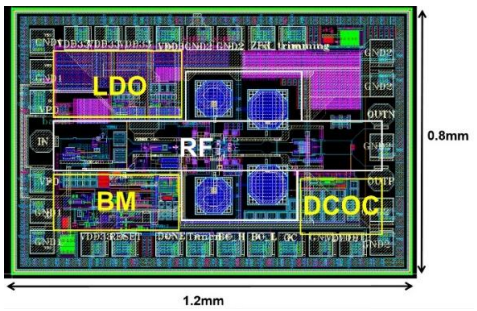


Fig. 8. Overall layout of BM-TIA.

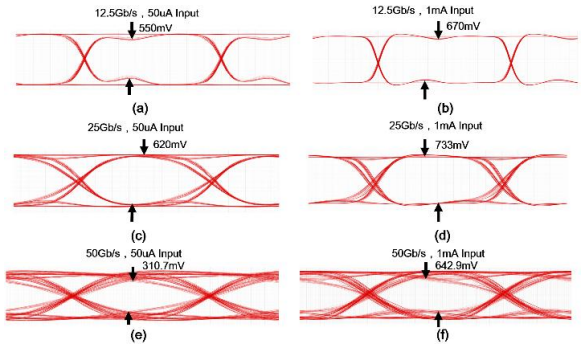


Fig. 9. The simulated eye diagram of (a) 50uA 12.5Gb/s, (b)1mA 12.5Gb/s, (c) 50uA 25Gb/s, (d)1mA 25Gb/s, (e) 50uA 50Gb/s, (f)1mA 50Gb/s input.

III. Post-Layout Simulation Results

The proposed chip is implemented in a 90-nm SiGe BiCMOS process. As shown in Fig. 8, the total die area, including pads, is 0.96 mm^2. In high-gain mode (HG), the TIA achieves a transimpedance gain of 82 dBΩ, while the low-gain mode (LG) provides 61.5 dBΩ. The simulation results show that the 3-dB bandwidth reaches 38 GHz in HG mode and 42 GHz in LG mode, which is sufficient for 50-Gb/s NRZ data transmission. Simulated eye diagrams (Fig. 9) confirm high signal integrity at 50 uA and 1 mA across all rates. Burst-mode evaluation (Fig. 10) shows that for a worst-case 2-mA input, the pulse-accelerated AOC loop completes settling within 6.5 ns. The BM_END signal marks the successful conclusion of the transient response.

Table I provides a comprehensive comparison between this work and state-of-the-art optical receiver front-ends reported in recent years. As summarized in the table, while there is a slight trade-off in noise performance to accommodate the wide dynamic range, the proposed design exhibits significant advantages in both bandwidth and settling time over existing solutions. Furthermore, this work demonstrates robust potential for 50G-PON applications. To the best of the authors' knowledge, this is the first burst-mode TIA to support triple-rate operation for 50G-PON while simultaneously achieving the shortest reported settling time.

IV. Conclusion

This 50G-PON BM-TIA features a merged approach for low-gain and rate-specific scaling for high-gain modes to reduce parasitic capacitance. By employing a concurrent OC scheme to activate AOC and ROC loops in parallel, the design achieves ultra-fast settling. Post simulations demonstrate an IRN current density of 14.8 pA/√Hz in HG mode, and a maximum settling time of 6.5 ns.

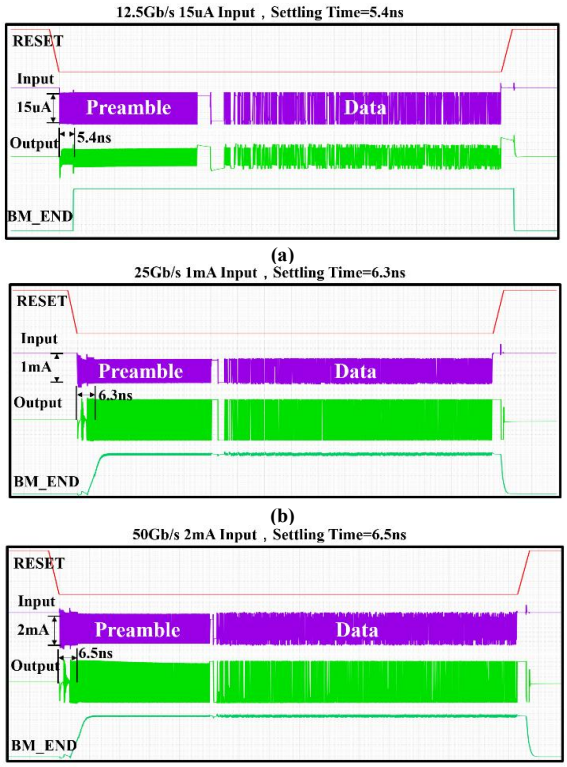


Fig. 10. Simulated burst mode response for (a) 12.5Gb/s 15uA input, (b) 25Gb/s 1mA input, (c) 50Gb/s 2mA input.

TABLE I. PERFORMANCE COMPARISON WITH PRIOR WORKS

Parameters	[11]	[12]	[13]	[10]	This work*	
	CICC 22'	OFC 23'	JLT 23'	CICC 25'	High Gain	Low Gain
Technology	40nm CMOS	0.13μm SiGe BiCMOS	0.13μm SiGe BiCMOS	28nm CMOS	SiGe BiCMOS	
Baud Rate (Gb/s)	10/2.5	25/12.5	50	50	**50/25/12.5**	
BW(GHz)	N/A	9.5	17.1	27	**38/13/7**	**42**
Gain(dBΩ)	N/A	58	80	67	**82/85/86**	**61.5**
Noise (pA/$\sqrt{Hz}$)	7.9/4.0	N/A	N/A	7	14.8/11.2/6.7^	49.5
Settling Time(ns)	16~37	200	150	14.7	**5.4/6.3/6.5**	
Dynamic Range(dB)	25.5/ 27.4	/	21.7	/	23.23/24.11/24.85	
Power(mW)	66	/	285	97.4	290.4	
Die Area(mm^2)	/	/	2.04	0.8	0.96	

*Simulation, ^ The equivalent input noise was integrated to 1.78 BW (the noise bandwidth of the second-order Bezier response)

Acknowledgment

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