A Low-phase-error FD-fNIRS Readout Circuit with Sub-1V Transimpedance Amplifier and LC-ADC-based Amplitude Control Loop

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***Abstract*—Frequency-domain functional near-infrared spectroscopy (FD-fNIRS) ultilizes the propagation time and amplitude attenuation of light in tissue to quantify blood oxygen concentration. This enables more detailed monitoring of human brain activity, providing a potential solution for non-invasive and wearable brain-computer interface (BCI) devices. However, the amplitude-phase coupling effect of the comparator in the phase detector introduces phase errors, which in turn leads to inaccuracies in the measurement of light propagation time. To suppress amplitude-phase coupling effect, an amplitude control loop based on the level-crossing analog-to-digital converter (LC ADC) is employed. The utilization of the LC ADC eliminates the need for a high-speed envelope detector, thereby reducing circuit complexity and power consumption. In addition, a sub-1V transimpedance amplifier (TIA) is employed to improve energy efficiency. The proposed structure achieves a phase error of 0.11° and 12 mW power consumption.**

***Index Terms*—Frequency-domain functional near-infrared spectroscopy (FD-fNIRS), amplitude control loop, level-crossing analog-to-digital converter (LC ADC).**

I. Introduction

The non-invasive and portable brain-computer interface is of great importance in the areas of cognitive neuroscience, clinical medicine, man-machine interactive, functional brain imaging, etc [1], [2]. Functional near-infrared spectroscopy (fNIRS), which is based on optical methods, provides an ideal solution for this purpose [3]. fNIRS offers better spatial resolution than electroencephalography (EEG), and is more cost-effective and portable than magnetic resonance imaging (MRI) [4], [5].

Continuous-wave fNIRS (CW-fNIRS) operates by detecting only changes in the intensity of near-infrared light passing through brain tissue, enabling it to measure relative changes of reduced scattering coefficient ($\mu_s^{'}$) and absorption coefficient (μ_a), then the concentration changes of oxygenated hemoglobin (HbO) and deoxygenated hemoglobin (HbR) can be derived [6]. However, CW-fNIRS lacks the ability to quantify absolute hemoglobin concentrations, cannot provide any information about the time-of-flight of photons through the tissue. In contrast, FD-fNIRS overcomes these limitations by simultaneously measuring the intensity and phase shifts of modulated near-infrared light through the human brain [7]. This capability allows FD-fNIRS to calculate absolute concentrations of HbO, HbR, and total hemoglobin (tHb), which is critical for quantitative analysis of human brain activity levels [8]. FD-fNIRS enables direct comparability of data across individuals and time, greatly enhancing the scientific rigor and reproducibility of research findings [9].

A typical FD-fNIRS system consists of source optodes and detector optodes [10], [11]. Each source optode comprises a laser diode and corresponding driver circuit. The driver circuit generates a high-frequency (10 MHz $\sim$ 100 MHz) modulated current to drive the laser diode, which in turn produces high-frequency modulated light [3]. In the detector optode, TIA directly processes the high-frequency modulated photocurrent signals, so it dominates the power consumption of the circuit [12]. Besides the power consumption, another key challenge is the accurate measurement of phase. The phase shift measurement accuracy of the emitted light directly affects the accuracy of $\mu_s^{'}$ and μ_a [13]. Unfortunately, the amplitude-phase coupling effect of the phase detection circuit introduces phase error.

In this paper, an amplitude control loop based on the LC ADC is proposed to suppress the amplitude-phase coupling effect of the phase detection circuit. In addition, to improve the energy efficiency of the FD-fNIRS chip, a low-voltage-supply (sub-1V) TIA is employed.

The rest of this paper is organized as follows. Section II presents the proposed architecture and operating principles is described in detail. Section III shows simulation results. Finally, Section IV concludes this paper.

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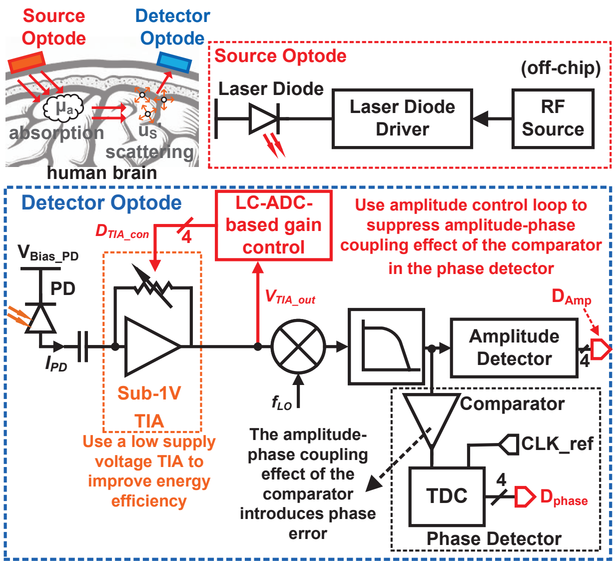

Fig. 1. Block diagram of the proposed FD-fNIRS readout circuit.

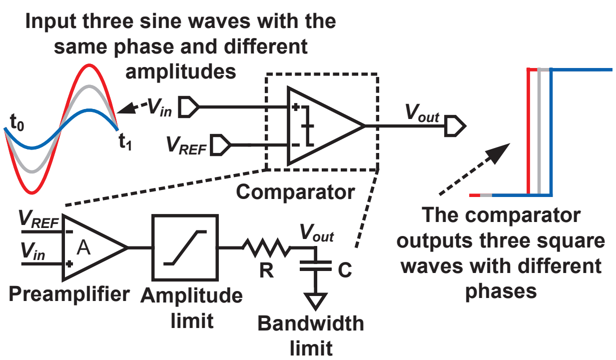

Fig. 2. The amplitude-phase coupling effect in the comparator.

II. Proposed Structure

Fig. 1 shows the proposed FD-fNIRS readout circuit based on heterodyne measurement.

In the phase detector, a zero-crossing comparator is first used to convert the sinusoidal signal into a square wave. Then, a time-to-digital converter (TDC) is employed to count the interval between the two edges—where counting starts when the reference clock edge arrives and stops when the measured signal edge arrives [14]. The count value directly represents the phase shift. In the comparator, the amplitude of the input signal varies with the metabolism of human tissues. Due to the finite gain-bandwidth product (GBW) of the comparator, signals with the same phase but different amplitudes will result in outputs with different phases after passing through the comparator, thereby introducing phase errors, as shown in Fig. 2.

The comparator is modeled as a cascade of the preamplifer stage, the amplitude-limiting stage, and the bandwidth-limiting stage [15], [16]. The sine wave at the moment it crosses the comparator reference voltage can be approximated as a ramp signal. Therefore, the delay phase of the comparator can be obtained by using Laplace transforms on a ramp signal applied to the transfer function of the RC network. Through theoretical derivation, the phase error of the comparator can be calculated using the following formula:

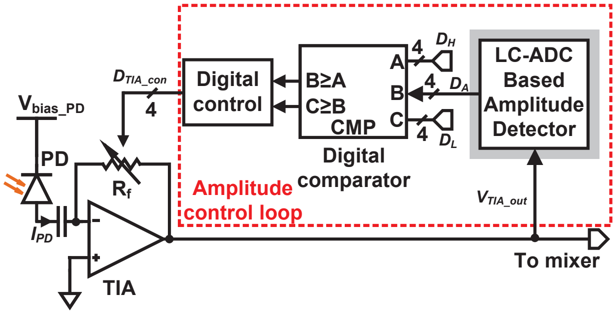

Fig. 3. Block diagram of the amplitude control loop based on LC ADC.

$$\phi_{error} = \frac{180°}{\pi}\sqrt{\frac{V_{DD}\omega_{in}}{\pi V_{\mathrm{REF}}\mathrm{GBW}}}\left(1-\sqrt{\frac{V_{\mathrm{REF}}}{V_{\mathrm{in}}}}\right) \tag{1}$$

where V_{in}, V_{REF} and V_{DD} are the amplitude of input signal, reference voltage of the comparator, and supply voltage of the comparator, respectively, ω_{in} is the angular frequency of the input signal, GBW is the gain-bandwidth product of the comparator. For instance, when a 0.8 V, 10 MHz sinusoidal wave passes through a comparator with a 1-GHz GBW, a phase error of approximately 0.13° is induced, casuing 12% measurement error of $\mu_s^{'}$ and μ_a [17].

To suppress the amplitude-phase coupling effect in the comparator, the proposed structure introduces an LC-ADC-based amplitude control loop before mixer, as shown in Fig. 3. An envelope detector cascaded with a Nyquist ADC can also digitize the amplitude of the signal. Envelope detectors can be implemented based on the charging and discharging of a capacitor. However, the envelope will exhibit sawtooth-like ripples with the same frequency as the input signal, which need to be filtered out by a subsequent-stage filter [18]. Furthermore, the input of envelope detector is a high-frequency modulated signal. To detect the amplitude of this high-frequency signal, the circuit requires careful optimization. This not only renders the envelope detector complex but also increases its power consumption. Instead, a LC ADC is used as an amplitude detector to digitalize the output of TIA, avoiding the use of envelope detectors. The digital comparators following the LC ADC judge whether the output of the LC ADC falls between D_H and D_L. If the output of the LC ADC is greater than D_H or less than D_L, the digital logic will decrease or increase the gain of the TIA by one step, respectively. By repeating the above procedures, the output of the TIA will stabilize between D_H and D_L, thereby reducing the amplitude-phase coupling effect of the comparator.

Fig. 4 and Fig. 5 show the block diagram of amplitude detector based on LC ADC and waveforms of key nodes, respectively. The operating principle of the circuit is explained

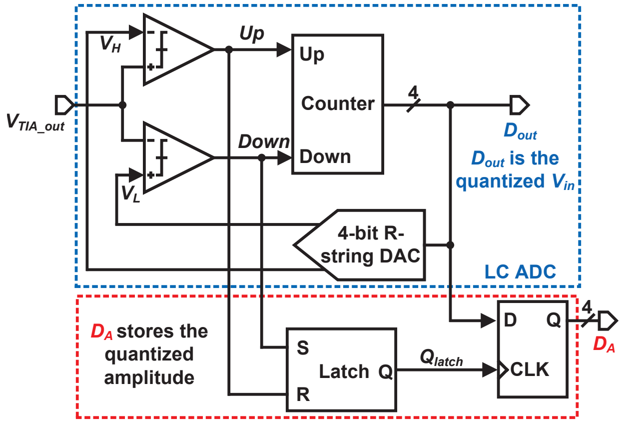

Fig. 4. The amplitude detector based on LC ADC.

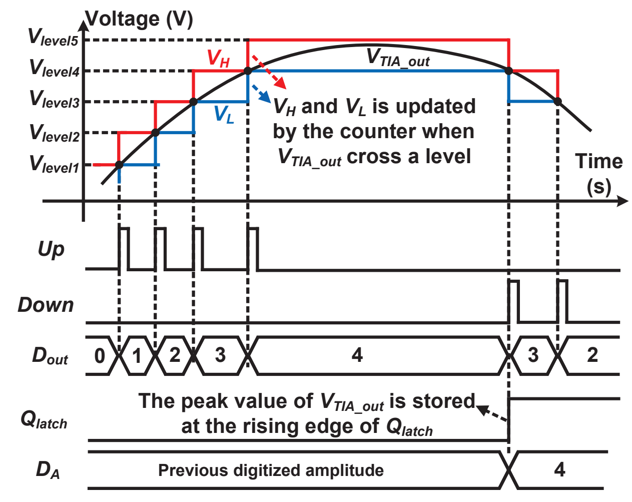

Fig. 5. Timing diagram of the amplitude detector based on the LC ADC.

as follows. The input signal (namely the output of TIA) V_{TIA_out} is connected with two comparators. When V_{TIA_out} is larger than V_H or less than V_L, Up and $Down$ will generate a pulse, respectively. A pulse on Up or $Down$ will make the counter increment by 1 or decrement by 1. Then, V_H and V_L is updated by a digital-to-analog converter (DAC), which is driven by the output of the counter. The SR latch receives the Up and $Down$ signals and outputs Q_{latch}, which indicates whether V_{in} is in a rising state or a falling state. The peak value of the signal occurs at the moment when the signal changes from rising to falling. That is, Q_{latch} changes from a low level to a high level at this moment. The value of D_{out} read at the rising edge of Q_{latch} is the digitized amplitude of V_{TIA_out}.

Besides introducing an amplitude control loop to suppress the amplitude-phase coupling effect of the comparator, a low-voltage TIA is also employed to improve energy efficiency [19]. Fig. 6 shows the TIA circuit and its equivalent model. From the equivalent model of TIA, we can get

$$\frac{V_{out}}{i_{in}} = -\frac{R_f A_i - R_{in}}{1 + A_i} \approx -R_f \tag{2}$$

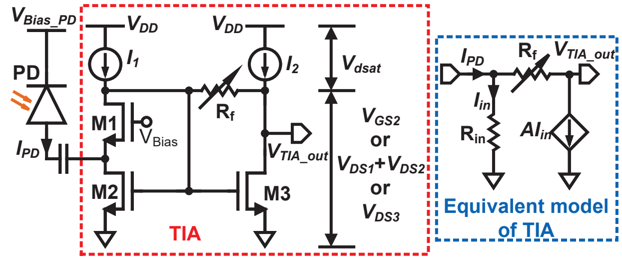

Fig. 6. The schematic of the sub-1V TIA and its equivalent model.

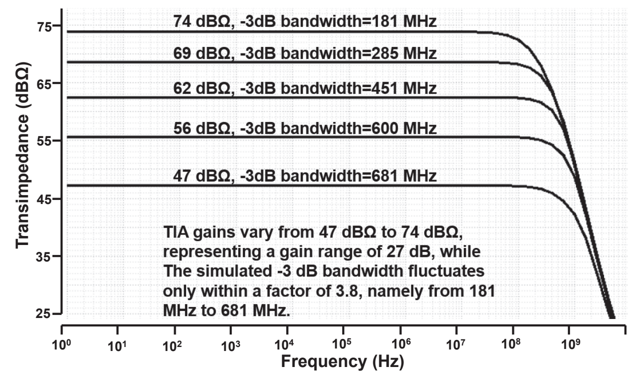

Fig. 7. Simulated frequency response of the sub-1V TIA.

where A is the current gain, R_{in} is the current amplifier's input resistance, namely $g_{M3}/[(g_{M2} + g_{M3})g_{M1}]$, which is negligible compared with $R_f A_i$. The TIA in Fig. 6 has the same transimpedance gain as the traditional TIA based on a voltage amplifier. Since the supply voltage is equal to an overdrive voltage plus the gate-source voltage, this TIA can operate in the low-voltage region. In this paper, the supply voltage is set to 0.9 V.

Furthermore, R_f in the TIA shown in Fig. 6 has no impact on the loop gain. Thus, the transimpedance gain is independent of the bandwidth. In contrast, in traditional voltage-amplifier-based TIAs, the feedback resistor R_f is responsible for converting the output voltage of the voltage amplifier into a current. Thus, R_f exerts an influence on the loop gain, which in turn affects the -3 dB bandwidth of the TIA. Specifically, as R_f increases, the -3 dB bandwidth of the TIA decreases. In circuit design, it is necessary to ensure that the bandwidth remains greater than the required bandwidth even when R_f is maximized. This leads to unnecessary power dissipation when R_f is not at its maximum value. Since the bandwidth of the TIA in Fig. 6 is independent of the transimpedance gain, this unnecessary power dissipation is avoided. Fig. 7 shows the simulated frequency response of the TIA. When the TIA gain varies from 47 dBΩ to 74 dBΩ, the -3 dB bandwidth of the TIA varies only within a factor of 3.8, from 181 MHz to 681 MHz.

III. Simulated Results

The proposed FD-fNIRS structure is simulated in 180-nm CMOS process. The optical intensity of the laser diode is

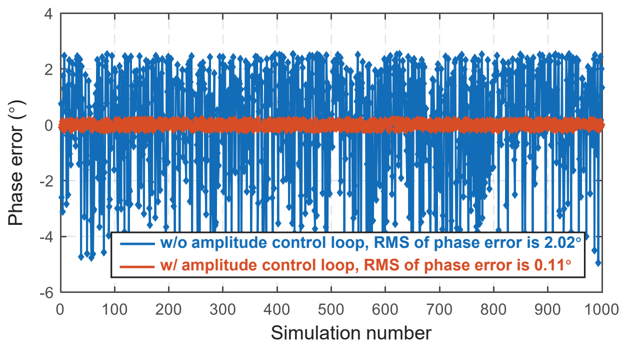

Fig. 8. Simulation results of phase errors with and without the amplitude control loop.

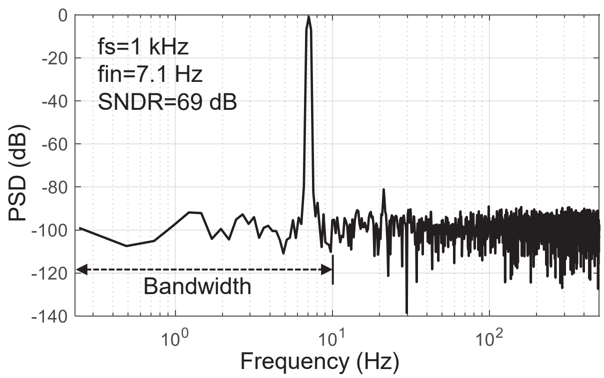

Fig. 9. PSD of SAR ADC.

modulated at 80 MHz. The local oscillation frequency of the mixer is set 80.01024 MHz.

The output of TIA varies randomly with the blood oxygen concentration in the human brain. Without the amplitude control loop, this random variable (namely the output of TIA) varies randomly within the output swing of the TIA (0.2V $\sim$ 0.8V). When the amplitude control loop is employed, the output of TIA is limited between 0.48 V and 0.52 V. Due to the amplitude-phase coupling effect of the comparator in the phase detector, random variations in amplitude introduce phase errors. In the two cases of with the amplitude control loop and without the amplitude control loop, 1000 random experiments were conducted respectively to observe the phase errors. Fig. 8 shows the simulated results. After employing the amplitude control loop, the RMS value of the phase error decreases to 0.11°. In comparison with the configuration without the amplitude control loop, the phase error is reduced by approximately a factor of 20.

The amplitude detector after the low-pass filter (LPF) adopts a cascaded structure of an envelope detector and a successive approximation register (SAR) ADC. Fig. 9 shows the power spectral density (PSD) of SAR ADC. When the sampling frequency is 1 kHz and the input signal is 7.1 Hz, the signal-to-noise and distortion ratio (SNDR) is 69 dB within the bandwidth ranging from 0 to 10 Hz. It should be noted that the amplitude detector in the amplitude control loop before the mixer is based on a LC ADC. This is because the signal before the mixer is a high-frequency signal, and the amplitude control loop based on the LC ADC avoids the use of the high-speed envelope detector, thereby reducing circuit complexity and power consumption. On the other hand, after the mixer, the cascaded structure of an envelope detector and a SAR ADC is adopted. This because the precision of LC ADC is typically lower than 6 bits [20], [21], which fails to meet the requirement for accurate amplitude measurement. After the signal passing through the mixer and the low-pass filter, only the low-frequency component is retained. For this low-frequency signal, the envelope detector can be easily implemented, and its power consumption is not high.

TABLE I
PERFORMANCE SUMMARY COMPARED WITH THE STATE-OF-THE-ART WORKS

Publication	[22]	[23]	[24]	This work
fNIRS Technology	FD	FD	FD	**FD**
Modulation Frequency	105 MHz	80 MHz	80 MHz	**80 MHz**
Technology	180 nm	130 nm	130 nm	**180 nm**
Power Supply	1.8 V	1.8/1.2 V	1.5 V	**1.8/0.9 V**
Power Consumption	47.6 mW	18 mW	30 mW	**12 mW**
Phase Error	1.68°	0.5°	0.2°	**0.11°**
Dynamic Range	60 dB	60 dB	60 dB	**69 dB**

Table I shows the performance summary and comparison with state-of-the-art FD-fNIRS readout circuits. The amplitude control loop reduces the phase error to 0.11°. Also, it shows a good power consumption of 12 mW.

IV. Conclusions

In this work, we propose a FD-fNIRS readout circuit with amplitude control loop to suppress phase error caused by the comparator in the phase detector. In the amplitude control loop, we use a LC ADC for amplitude detection to dynamically control the gain of the TIA. Using the LC ADC for amplitude detection eliminates the need for a high-speed envelope detector, thereby reducing the circuit complexity. In addition, a sub-1V TIA based on the current amplifier is employed to reduce power consumption. Another advantage of this TIA is that its bandwidth is independent of its gain. Simulation results show that the proposed fNIRS readout circuit achieves a RMS phase error of 0.11° and a power consumption of 12 mW. Compared with prior work, the phase error is reduced by 1.8× $\sim$ 15×, and the power consumption is reduced by 1.5× $\sim$ 4×.

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