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A Reconfigurable Intracranial Multimodal Monitoring ASIC with on-chip PVT-Insensitive Waveform Generator

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***Abstract*—This work presents a reconfigurable multimodal ASIC capable of interfacing with different types of intracranial sensors. The ASIC comprises two main functional blocks: an on-chip waveform generator and a reconfigurable readout circuit. To acquire high waveform consistency, a PVT-robust and area-efficient waveform generator is implemented on chip. By reconfiguring the feedback network to either a switched-capacitor transimpedance amplifier (SC-TIA) or a capacitively coupled instrumentation amplifier (CCIA) topology, the readout circuit flexibly measures voltage, current, and impedance. A current scaling technique has been applied to the front-end of the sensing amplifier, enabling wide dynamic-range current sensing from picoampere to milliampere levels. The proposed ASIC has been validated in the Cadence Virtuoso Environment using a 180-nm CMOS process. The waveform generator produces five programmable voltage profiles with tunable potential window and frequency, while only consumes a power of 17 µW and area of 0.36 mm^2. The readout circuit provides a 15-pA resolution and 157-dB dynamic range (DR) for current sensing with >0.999 linearity.**

***Index Terms*—Electrochemical impedance spectroscopy, electrochemical sensing, potentiostat, traumatic brain injury, waveform generator.**

I. Introduction

Traumatic brain injury (TBI) caused by significant impacts to the head, such as falls, motor vehicle accidents or assaults, is one of the leading causes of death and disability worldwide [1], [2]. Such injury often elevates intracranial pressure (ICP) within the cranium due to increased volume of brain tissue, cerebrospinal fluid, and/or blood [3]. However, standalone ICP monitoring remains insufficient for clinical management of TBI patients due to ICP's non-specific manifestation for pathogenesis [4]-[7]. Therefore, incorporating additional biomarkers such as brain tissue partial pressure oxygenation ($PbtO_2$), cerebral temperature, and immune factors, enables early detection and prevention of secondary brain injury, emphasizing the need for multimodal monitoring in TBI management.

Commonly applied approach for monitoring ICP or cerebral temperature is by acquiring voltage changes from a Wheatstone bridge with embedded pressure/temperature sensors [8], while biochemical concentrations, such as oxygen for $PbtO_2$, are typically quantified by measuring electrochemically induced faradic current [9], such as by chronoamperometry (CA), cyclic voltammetry (CV), fast-scan cyclic voltammetry (FSCV), square wave voltammetry (SWV), or differential pulse voltammetry (DPV). Given the diverse sensing modalities involved, a front-end that can measure current, voltage, and impedance is highly desirable.

Several integrated circuits have been developed [10]-[13] to support multi-modal measurements in TBI monitoring. However, many of them utilize dedicated readout circuit blocks for sensing current, voltage and impedance, resulting in substantial static power consumption and increased chip area. To optimize energy and area efficiency, a tri-mode readout architecture that can be reconfigured to meet the different sensor inputs. Although the readout circuits in [13] were highly integrated, the system relied on bulky external instruments for generating excitation waveforms. The typical implementation of on-chip waveform generator is using a discrete digital-to-analog converter (DAC) [14]. However, the inherent nonlinearity of the clock-based DACs often leads to distorted excitation waveform. To avoid this issue, an integrator-based method was proposed [15]. It forms a periodic voltage ramp by integrating a constant current over a capacitor before reversing the current's polarity, and repeating the process. Either a large capacitor in nF range or a tiny current in pA range is required in order to generate a sub-Hz excitation waveform. Instead of using area-extensive capacitors, a sub-pA current has been derived from a multi-stage current divider which can significantly downscale a nA-size reference current [16]. However, the generation of identical currents for charging/discharging capacitor suffer from non-ideal reference voltages and resistors that are sensitive to process, voltage, and temperature (PVT) variations. The non-ideal factors can significantly degrade the measurement accuracy.

In this paper, a reconfigurable intracranial multimodal monitoring ASIC has been proposed, which features five different types of excitation waveforms and supports voltage, current and impedance measurement. The proposed current reference used to produce triangular waveform is temperature-compensated with a tuning network, achieving a high PVT independence. This paper is organized as follows: Section II presents the detailed circuit implementation of the core blocks. Section III shows the simulation results and comparison with prior arts, and Section IV concludes this paper.

II. Circuits Design

Fig. 1(a) shows the system architecture of the reconfigurable multimodal monitoring ASIC, which consists of a PVT-insensitive on-chip waveform generator

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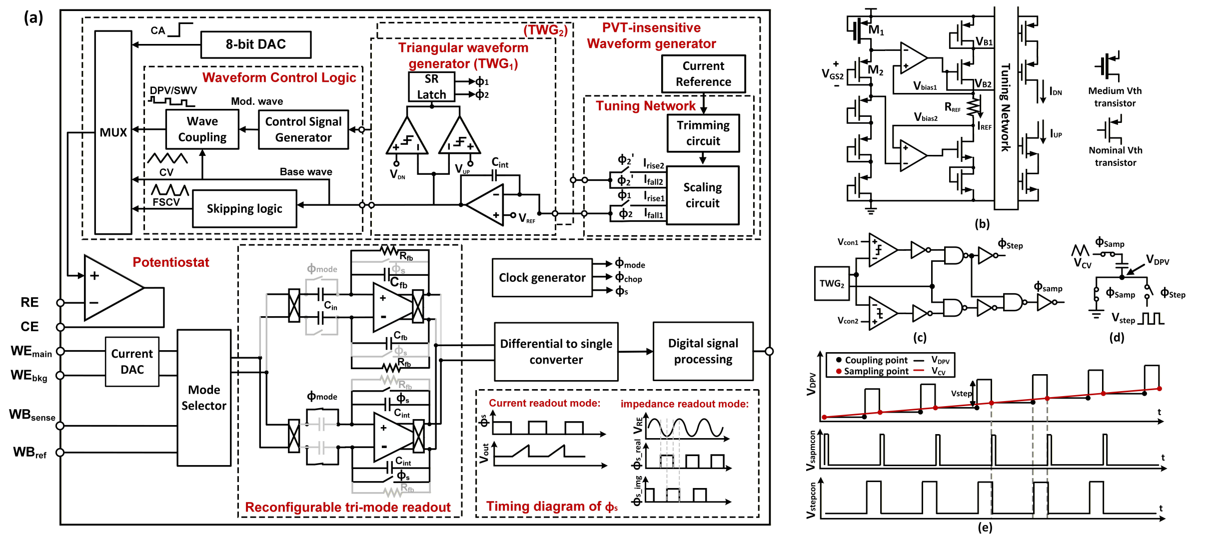

Fig. 1. (a) System architecture diagram of the intracranial multimodal monitoring system. (b) Schematic of the nA-size current reference with the following tunning network; (c) DPV control signal generation logic; (d) Waveform coupling scheme; (e) Signals for generation of DPV waveform.

(WG), a potentiostat and a reconfigurable tri-mode readout circuit. The waveform generator incorporates a current reference and a tuning network, along with two integrator-based triangular waveform generators controlled by waveform logic to produce the desired excitation signals. This excitation waveform across working electrode and reference electrode is maintained by the potentiostat, while the faradic current is measured by the readout circuit. By either tuning the reset-switch clock timing or reconfiguring the readout front-end, the system also supports impedance and voltage measurements. The differential output signal is converted into a single-ended signal and subsequently processed by the following feature-extraction circuits.

A. On-chip waveform generator

The schematic of the current reference is presented in Fig. 1(b). The current reference is generated by applying two reference voltages, V_{bias1} and V_{bias2}, across R_{REF} through two buffers. Additional diode-connected PMOSs are cascaded to ensure proper static operating point for these two buffering loops [17]. With the obtained V_{GS2} (=V_{bias1}-V_{bias2}) of about 130 mV in typical corner, a compact resistor in MΩ size can be realized to yield a sub-nA reference current. The temperature coefficient of V_{GS2}, TC_{VGS2}, is obtained:

$$TC_{V_{GS_2}}=TC_{VT}\cdot \ln\left(\frac{\mu_1\cdot Cox_1\cdot\left(\frac{W}{L}\right)_1}{\mu_2\cdot Cox_2\cdot\left(\frac{W}{L}\right)_2}\right)+ \frac{TC_{\mu_1}\cdot\mu_2\text{-}\mu_1\cdot TC_{\mu_2}}{TC_{\mu_1}\cdot TC_{\mu_2}}+(TC_{V_{th_2}}\text{-}TC_{V_{th_1}}) \quad (1)$$

where TC_x represents the temperature coefficient of parameter x; V_T is the thermal voltage; μ_n, C_{oxn}, $(W/L)_n$, V_{thn} are the carrier mobility, gate-oxide capacitance density, aspect ratio, and threshold voltage of M_n. By optimizing the size ratio of M_1 and M_2, an appropriate TC_{VGS2} can be obtained to compensate the temperature dependency of the reference resistor R_{REF}, thus achieving a near-zero temperature efficient of the reference current, I_{REF}.

The reference current, I_{REF}, was then fed into the following current mirror-based tuning network consisting of a trimming circuit and a scaling circuit. The former is employed to calibrate the I_{REF} to 2 nA with 6-bit resolution, effectively compensating for residual variation due to process and supply voltage. The trimmed current is then steered to a down-scaling circuit, achieving an output current range from sub-pA to nA level. For precise current-scaling ratio, especially for ultra-small currents, PMOS with thick gate oxide are utilized for switches in current mirrors due to its low leakage current. As shown in Fig. 1(a), the currents from the tuning network, I_{rise} and I_{fall} are utilized to charge/discharge the capacitor of subsequent two triangular waveform generators (TWG), inc. TWG_1 for the generation of base wave and TWG_2 for the modulation wave. This temperature-compensated topology with a tuning network ensures that I_{rise} and I_{fall}, despite fluctuations induced by PVT variations, remain highly stable. As I_{rise} and I_{fall} are generated from the same current reference, symmetric rising and falling slopes of the triangular waveform are inherently guaranteed with good matching.

The five voltage profiles for electrochemical excitation are produced as follows: while in the CV and FSCV modes, TWG_1 generates the required triangular waveform, in FSCV mode, an extra counter-based skipping logic is employed to insert specific periodic intervals between adjacent triangular waveforms. In the DPV mode, the fast modulation wave generated by the TWG_2 is applied to the input of two comparators in Fig. 1(c), to produce sampling and coupling control signals, $\phi_{Samplecon}$ and $\phi_{Stepcon}$. The control signals for generating DPV waveforms are shown in Fig. 1(e). By applying the control signals to the wave coupling scheme (see Fig. 1 (d)) as reported in [16], the coupling between the slow triangular base wave and the fast square modulation wave is achieved. The pulse width of $\phi_{Stepcon}$, which is related to the width of modulation pulse in the DPV waveform can be tuned by varying the comparator's input reference voltage, V_{con1}. V_{con2} are used

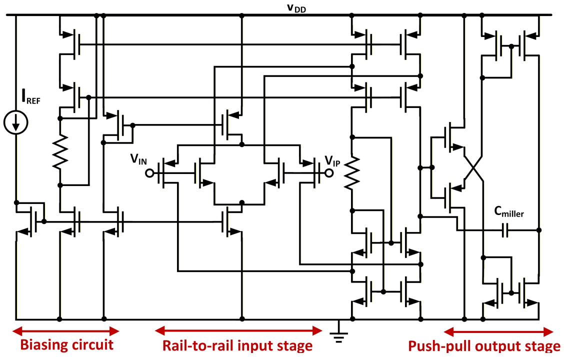

Fig. 2. The schematic of amplifier for potentiostat.

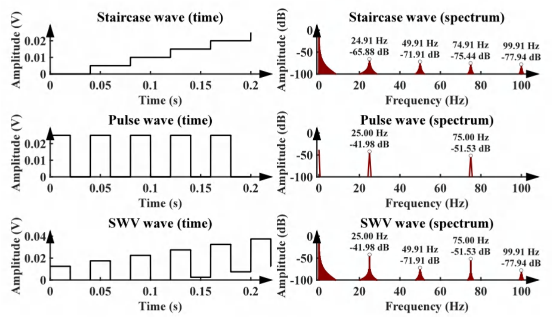

Fig. 3. DFT analysis of staircase wave, pulse wave, and SWV wave.

to generated the sampling pulse signal, $\phi_{Samplecon}$. Different from DPV mode, ϕ_1 of TWG_2 is used as the coupling signal to generate SWV waveform. In addition, in the CA mode, the output of a R2R DAC is applied to generate constant voltage profiles.

B. Potentiostat

To ensure a wide voltage swing and strong driving capability across varying dynamic-range loads, the potentiostat (see Fig. 2) adopts a self-biased rail-to-rail design with a common-source push-pull output stage. The driving capability of the amplifier is enhanced by increasing the aspect ratio of the output transistor to 8040μm/0.3μm. To ensure the loop stability of the potentiostat, a Miller capacitor of 6 pF is inserted to sufficiently separate the dominant pole from the non-dominant poles.

To determine the bandwidth of the potentiostat, typical frequencies and potential windows of different electrochemical excitation waveforms are summarized in Table I. The low-pass filtering process with a typical frequency was simulated using Discrete Fourier Transform (DFT) in MATLAB. Unlike CV or FSCV, where the outcome is obtained by analyzing a continuous waveform over at least one full cycle, SWV derives its outcome from measurements taken within the central interval between consecutive edges, as the sampling in practice occurs 1-2 ms before the end of each pulse [18]. Simulation results for various waveforms indicate that a maximum bandwidth of 12 kHz is required for accurately buffering SWV waveform, as presented in Fig. 3.

C. Reconfigurable multimodal readout circuit

In this paper, we introduced a tri-mode reconfigurable readout circuit, which can be operated as either a SC-TIA topology for current and impedance measurement under

TABLE I
WAVEFORM SETTINGS IN THIS WORK

Waveform	Voltage Range (V)	Wave Frequency (Hz)
CA	0 - 1(V_{RE})	dc
DPV [17]	Modulation Pulse: 12.5m	2
	Base Wave: 0.6 - 1.3(V_{RE})	0.007 @ (0.7 V, 0.01 V/s)
SWV [18]	Modulation Pulse: 12.5m	25
	Base Wave: 0.6 - 1.3(V_{RE})	0.093 @ (0.7 V, 0.13 V/s)
CV/FSCV [10], [16]	0.9 - 1.5(V_{RE})	416.7 @ (0.6 V, 520 V/s)

different resetting clocks, or a CCIA topology for voltage measurement. The fully differential topology utilized in the readout circuit, provides high rejection for common-mode interference, such as the reference voltages in the Wheatstone bridge and the background currents inherent in electrochemical sensing. An 8-bit current-mode DAC is utilized for current scaling with binary weighting prior to the readout circuit to improve the DR.

The SC-TIA is chosen due to its inherent bidirectional measurement property, which is particularly beneficial for electrochemical applications; high gain flexibility by simply adjusting the frequency of the reset clocks; as well as the intrinsic low-pass filtering effect during the integration, which eliminates the high-frequency noise from the sensing electrode. The circuit operates in two periodic phases:

i) during the first phase when ϕ_s is open, the input current is integrated across the C_{int};

ii) in the subsequent phase, the reset switch closes to prevent C_{int} saturation. The I-V characteristic of the current-mode SC-TIA can be expressed as:

$$V_{out}=\frac{I_{main}-I_{bkg}}{f_s\cdot C_{int}} \qquad (2)$$

where I_{main} and I_{bkg} are the input sensing current and background current, respectively; f_s is the frequency of resetting switches; and Cint is the feedback capacitor of the SC-TIA. The SC-TIA topology utilized a single-stage folded-cascode amplifier due to its high gain, high stability and short settling time. Its input pair is realized by PMOS with a large aspect ratio in order to reduce the flicker noise and transistor mismatch. Chopper stabilization technique is employed to further reduce the flicker noise and eliminate the DC offset. The chopping frequency is required to be much larger than the $1/f$ noise corner frequency and smaller than the reset switching frequency; therefore, it is set to 10 kHz. The capacitance of the feedback capacitor is set to be 5 pF due to the trade-off between gain ratio and area overhead.

Conventional electrochemical impedance spectroscopy (EIS) readout circuits operate by applying a small-amplitude AC excitation voltage to the potentiostat, measuring the resulting current response, and then extracting the real and imaginary components of the impedance via demodulation techniques. The demodulation is typically achieved by two mixers and LPFs, resulting in high power consumption and area overhead. The SC-TIA serves as a mixer under proper selection of the phase of the reset switching clock, as described in [20]. The real and imaginary components of

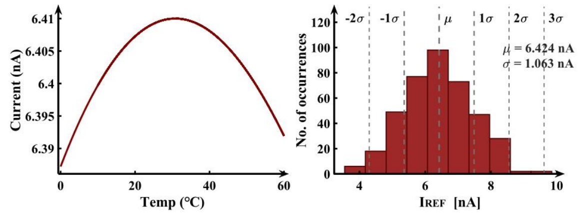

Fig. 4. (a) Post-layout simulation results of the reference current versus temperature, (b) Monte-Carlo simulation of I_{REF} @ 37°C.

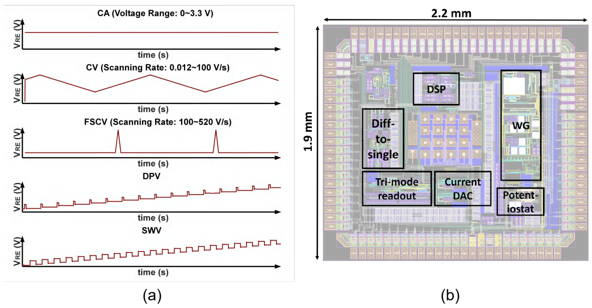

Fig. 5. (a) Simulated excitation waveform of CA, CV, FSCV, DPV and SWV;(b) Layout of the intracranial multimodal monitoring ASIC.

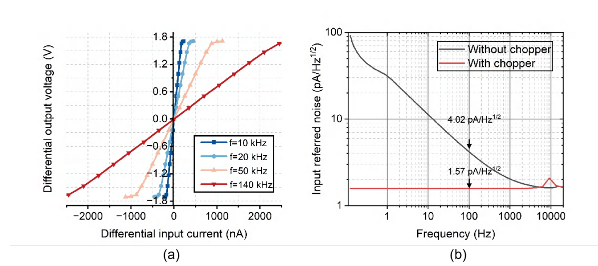

Fig. 6. (a) I-V characteristics of the readout circuit with different clock frequencies; (b) input referred noise with and without chopper.

TABLE II
COMPARISON WITH READOUT ASICS

	TBCAS [16]	TBCAS [13]	JSSC [23]	This work*
Supply (V)	1.2	1.2	1.8	1.8
Readout Circuit in SC-TIA mode				
Modalities	I	I, V, R	I, V, T	(I, V, Z)[a]
Linearity (R^2)	0.995	>0.999	-	>0.999
Resol. (pA)	2	40.6	14	15.5
DR (dB)	130	52	114	157
Read. area (mm²)	1.5	0.5	0.22	0.12
Waveform Generator (WG)				
On-chip WG	Yes	No	No	Yes
EM supported	4	-	-	5
Scan rate (V/s)	0.08~400	-	-	0.012~520
WG power (µW)	25.3	-	-	17
WG area (mm²)	0.57	-	-	0.36

EM: Electrochemical methods; a: Reconfigurable topology; *: This work is based on post-layout simulation results.

the measured impedance can be derived as:

$$V_{\text{out\_real}}=-\frac{2A}{\omega\cdot C_f}\cos(\phi) \quad (3)$$

$$V_{\text{out\_img}}=\frac{2A}{\omega\cdot C_f}\sin(\phi) \quad (4)$$

where the differential faradic current for EIS measurement is supposed to be $Asin(\omega t+\phi)$. In the voltage mode, the readout circuit is reconfigured to a CCIA, which reuses the same feedback capacitor and amplifier as those in the SC-TIA. Because the ICP signal is of low frequency, from 0.05 Hz to a few Hz [21], the chopper is placed before the input capacitor to up-convert the baseband signal to around f_{chop} for subsequent amplification. To achieve the low cut-off corner of the high-pass filter, f_{HP}=1/(2π$R_{fb}C_{fb}$), the pseudo-resistors of high resistance are utilized in the feedback loop to set the DC bias.

III. SIMULATION RESULTS

Fig. 4 shows the post-layout simulation results of the current reference circuit in a 0.18-μm CMOS technology. When both process variation and mismatch are considered, the Monte Carlo distribution over 400 runs gives a mean temperature coefficient of 119.1 ppm/°C, providing robust temperature stability for excitation wavefroms. Fig. 5(a) presents the simulated results of five electrochemical excitation waveforms. The slowest and fastest ramps of 0.012 V/s and 520 V/s are achieved in the CV and FSCV modes, respectfully. The waveform generator exhibits a maximum power consumption of approximately 17 µW when generating a FSCV waveform with the fastest ramp. Based on the Randles equivalent circuit in [22], the potentiostat achieves bandwidths from 10.5 kHz to 14.4 kHz under various solution resistance [22] and double-layer capacitance [18], demonstrating adequate bandwidth for various electrochemical load.

The input-output characteristic of the readout circuit in the current mode is shown in Fig. 6 (a) with different clock frequencies, showing a linearity of R^2=0.999 for input currents up to ±2.1 µA at the clock frequency of 140 kHz. Benefiting from the 8-bit current-scaling circuit, which effectively reduces the input current amplitude, the readout circuit attains a high dynamic range of up to 157 dB. Fig. 6 (b) shows the periodically steady state noise simulation of the readout circuit when the input current is zero. The integrated input referred noise from 0.007 Hz to 100 Hz can be calculated to be 15.5 pA_{RMS} when the chopper is on and 102.1 pA_{RMS} when the chopper is off.

Table II shows the performance summary of the proposed ASIC. The on-chip waveform generator only occupies approximately 0.36 mm², achieving a 37% area reduction compared to [16]. The reconfigurable readout circuit achieved superior dynamic range of 157 dB, outperforming prior art.

IV. CONCLUSION

The paper presents a reconfigurable multimodal monitoring ASIC. A PVT-insensitive nA current reference is utilized for integration in the implementation of the on-chip waveform generator, achieving symmetric ramps and high area efficiency. By reconfiguring the feedback network, the readout circuit achieves multi-parameter sensing without using multiple dedicated readout branches. The DAC-based current-scaling architecture dynamically regulates input signal amplitude, enabling the readout circuit to achieve seven-order current detection capability spanning from picoampere-level to milliampere-level measurements with a wide dynamic range of 157 dB.

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